

InfoTracks

Semitracks Monthly Newsletter



Ion Implantation Part II – Process Issues

By Christopher Henderson

This month we continue our overview of ion implantation. This month we are addressing processing issues associated with ion implantation. To access Part I in last month's newsletter, click [here](#).

In this article, we will discuss charge neutralization, energy contamination, wafer charging, wafer heating, photoresist outgassing, implant angle effects, and ultrashallow junction formation.

The first process challenge we'll discuss is charge neutralization. We know that the ions need to maintain a specific charge state during the implant process. However, these ions can be neutralized by collisions with gas atoms in the chamber. This is a big problem during boron deceleration, which is used in some implant systems to create shallow junctions. Neutral atoms are a problem because they cannot be accelerated and steered properly with electrostatic plates. They will not be implanted to the correct depth if the neutralization occurs early on; they will not be spread uniformly across the wafer if the system employs electrostatic scanning, and they will not be counted by the dose measurement system.

A different problem happens at higher energies—collisions between ions and atoms can cause increased ionization. The solution is to remove, as much as possible, the atoms from the chamber. This means ultra high vacuum is required in the beamline and in the chamber. This in turn means that one must use high capacity pumps and perform frequent regeneration of cryopumps. One should also avoid decelerating the beam, and one should provide neutral traps or

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Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

beam filters to remove neutral species.

Charge neutralization brings up a broader issue, that of energy contamination. This situation occurs when ions of the wrong energy are implanted. This leads to incorrect doping profiles. The main causes are charge neutralization, which we discussed, and contaminants of the same mass-to-charge ratio not being removed by the mass analysis magnet. An example of this would be a double-charged dual phosphorus ion in a single-charged single phosphorus ion beam. One would use the same solutions for this problem as with charge neutralization.

Another concern is contamination control. Contaminants can come from apertures, wafer holders, and metals used in the beam line hardware. They can also come from other dopant atoms used in the system that have been implanted into the hardware and then resputtered. And they can come from particles of material flaked off from the beamline hardware or wafer handling system and then transported in the beam by the electrostatic forces. This problem can be minimized by routine cleaning of the components, using materials with low sputter yield in the beamline like carbon, and dedicating implanters by species to prevent cross contamination.

Another significant problem is wafer charging. This can result in device damage due to ESD as charge builds up in sensitive gates. It can also result in non-uniformity, due to the charge on the surface distorting the incoming beam. This is typically a problem with high current implanters. One solution is to use a system to reduce wafer charge. A common method is to use a plasma flood gun. This produces low energy electrons at the surface that can recombine with the charged ions. The goal here is to balance the charge and charge flow at the surface. Another solution is to minimize the beam density by employing dual mechanical or ribbon scanning methods, moving to batch processing to increase the implant area, and increasing scan speeds to lower dwell times. This reduces the time for charge buildup.

Another significant problem is heat generation. High-energy ions decelerate in the wafer, and much of that energy is dissipated as heat. This excess heat can damage photoresist masks, leading to critical dimension changes, or even blistering, flaking or popping. High temperatures can also lead to dopant redistribution, as diffusion processes accelerate exponentially at higher temperatures. This can also lead to undesirable forms of crystal defects. This is mainly a problem with high power, high mass implants where the energy dissipation is significant. The equation below helps to illustrate the dependence on both accelerating voltage and current.

$$P(\text{Watts}) = I(\text{mA}) \times V(\text{kV})$$

The solutions for this problem include proper wafer cooling, performing hard bake or other resist stabilization techniques, and minimizing the power density with larger beam sizes, faster scanning, and so on.

Still another problem is photoresist outgassing. Energetic ions will break the resist polymer bonds, releasing hydrogen. This problem is strongly related to beam power density. The increased heat makes the resist more susceptible to this problem. There are two main issues here. One is charge neutralization, and the other is resist mask damage. Liberated hydrogen will interfere with charge neutralization efforts. The solutions here are to optimize the resist process through hard bakes or ultraviolet photostabilization, increasing the equipment chamber size to reduce local hydrogen concentrations or use high pump speed vacuum systems, minimizing the beam power density, and conditioning the resist through a controlled ramp-up of beam current for example.

Implant angle effects also pose a challenge for process integration. There is beam shadowing that occurs in the channel from 7° implants, a common angle that helps minimize ion channeling. This leads to non-symmetrical channels under the mask edge. This can be addressed through quad implants or through zero degree implants. Some newer implanters can also achieve these effects through beam steering. Another implant angle effect is variation in implant angle in a batch processor. Wafers at the outside receive a different angle implant than those at the center. The solution here is to go to a single wafer implanter with parallel scan to minimize the effect.

Figure 1 groups most common implant applications together so that we can visualize the differences. The chart shows the applications as a function of energy and dose. We start with the highest dose, lowest energy implants, moving toward the lower dose, high energy implants. High current implants are typically done close to the surface, and are done later in the process, so one requires heavier doping to overcome the doping from previous implants. Medium current implants are performed to create the transistor wells and isolation regions, and to determine the transistor channel properties. High energy implants are done to create isolation regions, wells, and deep wells for some types of bipolar or BiCMOS transistors. They can also be used for charge-coupled device structures.

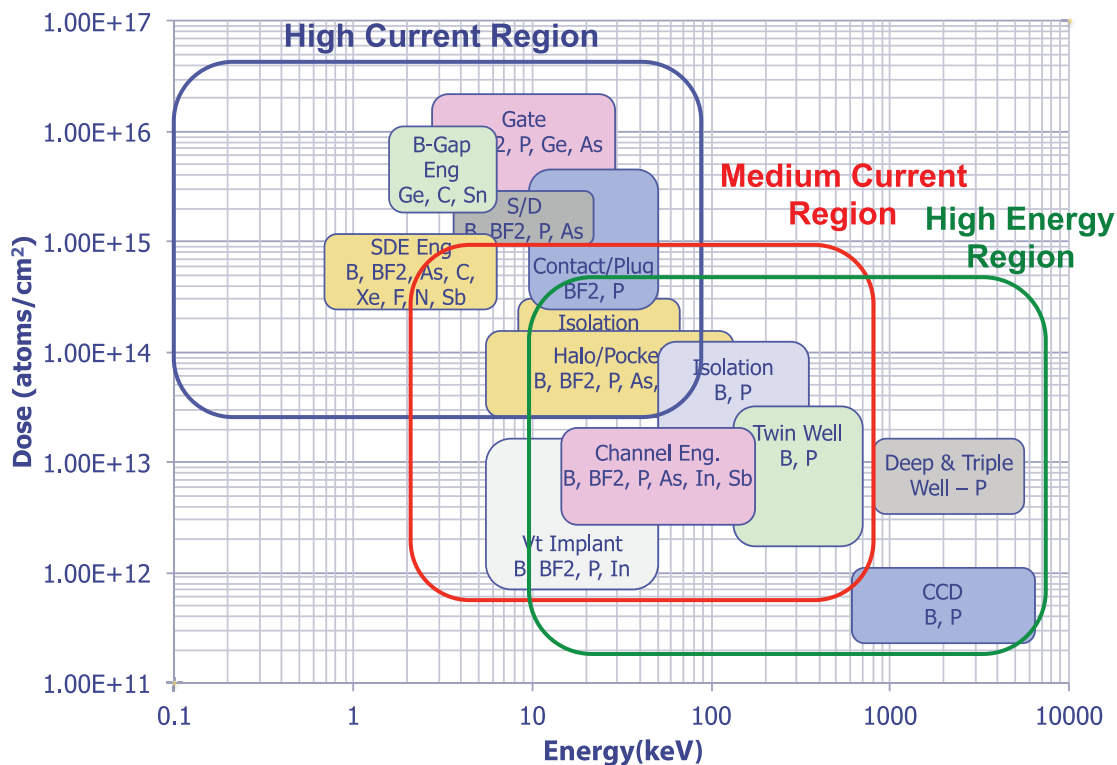


Figure 1: Chart showing applications as a function of energy and dose.

Medium current implants are used for both well and channel engineering. Channel engineering is used to control the drive characteristics of the transistor, and well engineering is used to control the isolation

between transistors. The three common channel engineering implants are the halo implant, the threshold adjustment implant, and the super steep retrograde or SSR implants. The three well engineering implants are for shallow wells, deep wells, and channel stops.

Some medium current implants, their dose ranges, energy ranges, and tilts are given in this table. Medium current implants can include layers done close to the surface, like halo implants or threshold adjust implants, or layers put in further below the silicon surface, like deep well structures.

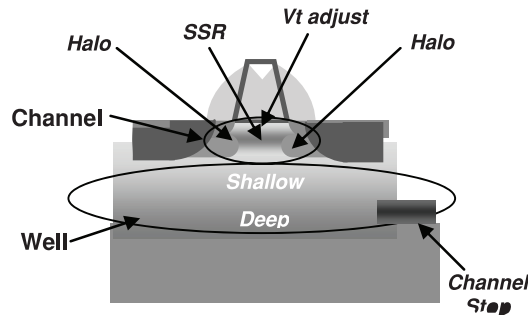


Figure 2: Applications for medium current implants.

Mid Current Implants			
Implant	Dose Range (cm ⁻²)	Energy Range (keV)	Tilt
Channel Engineering			
Halo	1e ¹³ – 6e ¹³	2 – 40	Yes
Vt	5e ¹¹ – 5e ¹²	5 – 40	No
SSR	5e ¹¹ – 8e ¹²	100 – 200	No
Well Engineering			
Shallow well	8e ¹² – 3e ¹³	100 – 600	No
Deep well	6e ¹² – 1e ¹³	800 – 1200	No
Channel stop	5e ¹² – 1e ¹³	80 – 200	No

Figure 3: Table showing typical energies and doses for medium current implants.

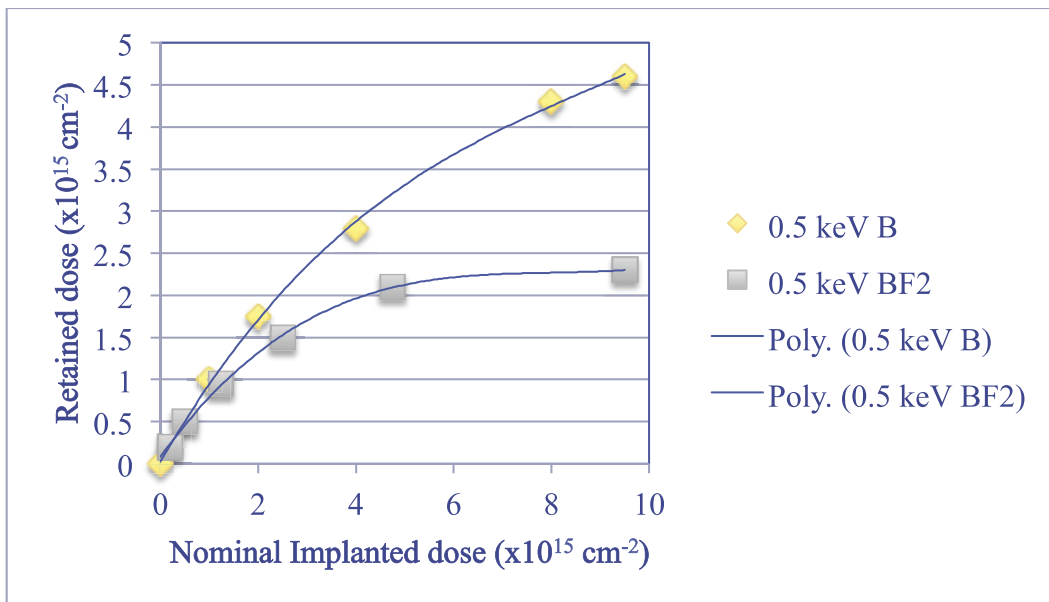
High dose applications are used for heavily doped regions. These include source-drain regions as well as their extensions, polysilicon gate doping, and pre-amorphization implantation.

High Dose Implants			
Implant	Dose Range (cm ⁻²)	Energy Range (keV)	Tilt
Source/Drain	8e ¹⁴ – 5e ¹⁵	1 – 5	No
SDE	5e ¹⁴ – 5e ¹⁵	0.2 – 5	Low
Gate Doping	5e ¹⁵ – 5e ¹⁶	2 – 5	No
PAI	5e ¹⁴ – 1e ¹⁵	10 – 30	No

Figure 4: Table showing typical energies and doses for high dose implants.

A final remaining challenge is ultra-shallow junction or USJ formation. Ultra-shallow junctions are critical for today's nanometer-scale ICs. The big challenge with ultra-shallow junctions is the boron implant. Boron is a small atom and is therefore easily accelerated in the beam that leads to a high projected range and straggle. To reduce this variability, low energies are required, so beam deceleration is used. Another challenge is low beam current. The need for beam deceleration leads to beam blow up that requires a lower beam current. Lower energies also cause increased sputtering of the silicon surface. Lower energies also lead to increase backscattering of boron atoms. At 500 volts, there is a 10% boron loss, and it increases to a 20% loss at 200 volts. Furthermore, these effects increase with accumulated dose. Finally, transient-enhanced diffusion creates problems, where the silicon damage leads to increased movement of boron atoms.

The goal with ultra-shallow source drain regions is to create 50 to 100 nm deep junctions and 30 to 60 nm junctions for the extensions with minimal dopant redistribution and residual damage. One method to do this is to implant boron difluoride (BF₂) instead of pure boron. This was a common technique in older processes and overcomes the deceleration problem, since the heavier molecule is not accelerated as much to begin with. However, the fluorine atoms contribute to boron sputtering.



This graph shows a retained boron dose versus a nominal boron dose in wafers implanted with either boron or BF2 at an equivalent boron depth. The trend lines are third order splinefits. For a nominal dose of one times ten to the fifteenth atoms per centimeter squared, the sputtering leads to a ten percent reduction in the retained dose for 500 volts or a twenty percent reduction at 2.2 keV BF2. Another solution is to improve boron transport efficiency by reducing beam blow up. One minimizes the beam path length to accomplish this. There is no deceleration post analysis as a result. Other approaches include electron confinement in the mass analysis magnet or using other beam focusing or shaping elements. A third approach is to use cluster boron beams; this topic is discussed in more detail on the Semitracks Online Training Website.

Technical Tidbit

Applications of the Coffin-Manson Model

Most of us are familiar with the basic Coffin-Manson model, but there are actually several variations to this model that can be quite useful. Read on for more details.

The basic Coffin-Manson model is shown here:

$$N_f = C_0 \times (\Delta T)^{-1/c}$$

where N_f is the number of cycles to fatigue, C_0 is a constant, ΔT is the temperature cycling ranging, and c is the Coffin Manson exponent. There are several other forms of the equation that are used to model failures in semiconductor components and electronic systems. We'll discuss these below.

Another version of the formula takes into account that there may be elastic as well as plastic deformation that occurs. Elastic deformation will not cause cracking; only plastic deformation does. Therefore, one should subtract the temperature range associated with elastic deformation out of the formula. One can modify the Coffin Manson model like this to take this into account:

$$N_f = C_0 (\Delta T - \Delta T_0)^{-1/c}$$

where ΔT_0 is the temperature range where elastic deformation occurs. The reason that one sees the main effect being low temperature is that $\Delta T - \Delta T_0$ is greater in this scenario. For example, let's assume that the elastic deformation region (ΔT_0) extends 50°C below neutral stress at 150°C, or to 100°C. If we temperature cycle from -55°C to +125°C, then $\Delta T - \Delta T_0$ is 155°. If we temperature cycle from 0°C to +125°C, then $\Delta T - \Delta T_0$ is only 100°. Therefore the minimum temperature has the most impact. Absolute temperature swings will also factor in as well.

Another form of the Coffin-Manson model is the Norris-Landzberg Model. It is used for modeling cracking on solder materials. It is written like this:

$$N_f = C_0 (\Delta T)^{-n} (f)^m \exp(E_a/kT)$$

The acceleration factor for the Norris-Landzberg model is given by:

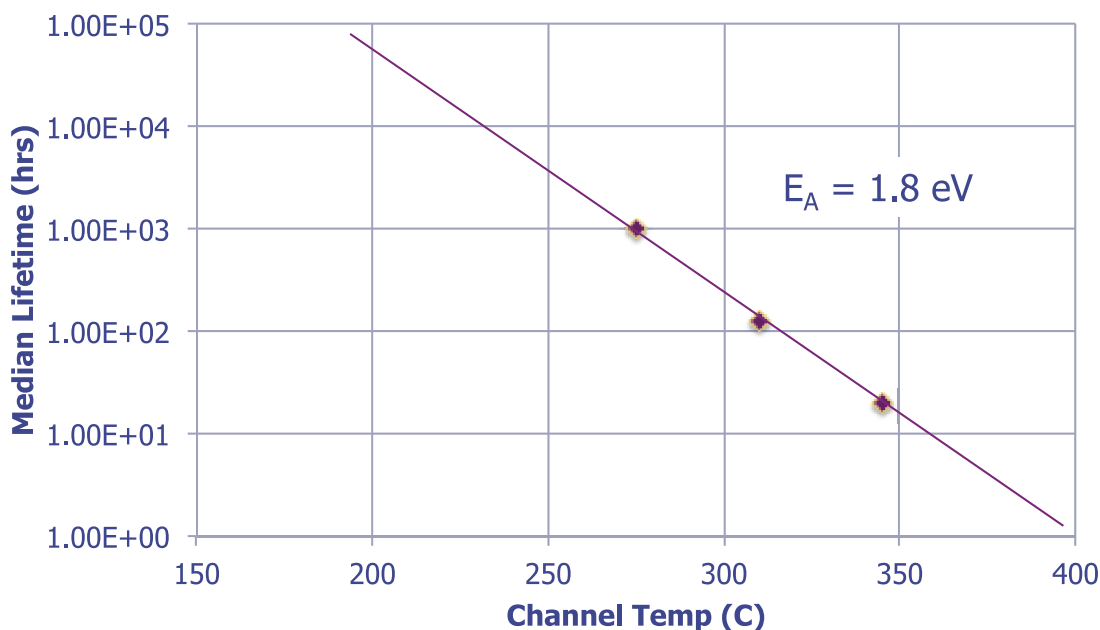
$$AF = \frac{N_f(USE)}{N_f(ACC)} = \left(\frac{\Delta T_{acc}}{\Delta T_{use}} \right)^n \left(\frac{f_{use}}{f_{acc}} \right)^m \exp \left[\frac{E_a}{k} \left(\frac{1}{T_{use}^{max}} - \frac{1}{T_{acc}^{max}} \right) \right]$$

The parameters for lead-tin solder are typically $n = 1.9$, $m = 0.33$, and $E_a = 0.122\text{eV}$. For lead-free solders, engineers typically use $n = 2.65$, $m = 0.136$, and $E_a = 0.189\text{eV}$.



Ask the Experts

Q: I have seen graphs (like I show in the graph below) where engineers have plotted median lifetime hours (log scale) as a function of temperature (linear scale), drawn a straight line through it, and then used the slope to determine the activation energy. Is this a correct way to calculate activation energy?



A: Normally, one would plot the temperature axis as one over T on a linear axis. By plotting T on a linear axis, you are not properly calculating the activation energy when drawing a straight line through the data.

Spotlight on our Courses: MEMS Technology

Our MEMS Technology Course will be offered in Enschede, Netherlands, June 12 – 13 this year. Here is more information about the course. If there is sufficient demand, we'll also offer it in the US later this year. If you're interested in having this course as an in-house course for your staff, please feel free to contact us at (505) 858-9813, or at info@semitracks.com.

OVERVIEW

Microelectromechanical Systems (MEMS) have captured the interest of the public with their promise to miniaturize existing systems. Although much of the excitement surrounding MEMS has died down, real applications are beginning to emerge. MEMS accelerometers for games, automotive, and wireless applications have emerged. MEMS inkjet chips are now ubiquitous, and new applications for RF and sensors are in development. One of the most challenging aspects of MEMS is packaging. Forces that normally do not affect meso-scale objects must be understood and controlled at the micro-scale. This has created a number of challenges related to the packaging of these components. *MEMS Technology* is a 2-day course that offers detailed instruction on the design, processing, packaging, and reliability of MEMS devices. We place special emphasis on DRIE, surface-to-volume ratio issues, electrostatics, liquid wetting, inertia, and other parameters. The course also contains a number of models and simulations used in conjunction with MEMS devices. This course is a must for every manager, engineer, and technician designing MEMS devices, using MEMS components in high performance applications or new packaging configurations, or supplying packaging tools to the industry.

By focusing on the fundamentals of MEMS devices and packaging, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain MEMS Technologies without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about these unique devices. This skill-building series is divided into three segments:

1. **Device Design and Processing.** Participants review the basic wafer processing steps for MEMS devices, including deep reactive ion etching, wet etching, patterning, CMP, and more.
2. **MEMS Packaging.** Participants learn the fundamentals of packaging concepts for MEMS devices. They learn about structural release, cleaning, encapsulation, and basic testing. They also discuss the challenges associated with packaging.
3. **MEMS Reliability.** Participants learn MEMS reliability issues and associated analysis and simulation techniques. They also learn about the physics and mechanics issues involved in reliability degradation of MEMS devices.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of MEMS and its technical issues.
2. Participants will learn the unique processing steps related to MEMS technology, including deep reactive ion etching, non-standard silicon orientation wafers, and special thin-films and coatings for moving components.

3. Participants will understand the basic concepts behind thermal and mechanical simulations of MEMS packages.
4. The seminar will identify the key issues related to the success of MEMS packaging. This includes the need for understanding charge, release, and package environments.
5. The seminar offers a wide variety of sample modeling problems that participants work in class to help them gain knowledge of the fundamentals of MEMS packaging.
6. Participants will be able to identify basic and advanced principles for mechanical stress, charge, and thermal diffusion.
7. Participants will understand how process, release techniques, and packaging are interrelated.
8. Participants will be able to make decisions about how to construct and evaluate new MEMS packaging designs and technologies.
9. Participants will also be introduced to wafer-level simulations, which are important to MEMS packages.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor packaging and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is application. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field.

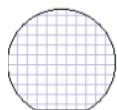
COURSE OUTLINE

1. Introduction to MEMS Technologies
 - 1.1. Basic Concepts
 - 1.2. MEMS-related Definitions
 - 1.2.1. MEMS Mechanics
 - 1.2.1.1. Mechanical/Thermal
 - 1.2.1.2. Microfluidics
 - 1.2.2. MEMS Physics
 - 1.2.2.1. Electrical/Optical
 - 1.2.2.2. Joule Heating
 - 1.3. From MEMS to NEMS
2. MEMS Device Design & Function
 - 2.1. Piezoelectric Inkjet Heads
 - 2.2. Accelerometers & Gyroscopes
 - 2.3. Flow & Pressure Sensors
 - 2.4. Micromachines & Micromotors
 - 2.5. Optical Display & Switching Devices
 - 2.5.1. RF-MEMS & MOEMS
 - 2.6. Designing & Simulating Operation
 - 2.7. Linear Actuation, Comb-Drive Actuation, & Resonators

3. MEMS Device Processing
 - 3.1. Lithography, Patterning, & Lift-off
 - 3.2. Etching
 - 3.3. Deposition
 - 3.4. Sacrificial & Structural Layers
4. MEMS Assembly, Packaging, & Testing
 - 4.1. Packaging Types & Options
 - 4.2. Structural Release
 - 4.3. Die Attach Process
 - 4.4. Interconnects
 - 4.5. Gettering
 - 4.6. Encapsulation & Capping
 - 4.7. When and How Should We Test?
5. MEMS Reliability
 - 5.1. Device-Level Failure Mechanisms
 - 5.1.1. Stiction (Release- or Shock-related) and Wear
 - 5.1.2. Particle Contamination
 - 5.1.3. Electrostatic discharge (ESD) & Electrical Overstress (EOS)
 - 5.2. Package-Level Failure Mechanisms
 - 5.2.1. Thermomechanical Stress & Fatigue
 - 5.2.2. Shock & Vibration
 - 5.2.3. Moisture/Corrosion
 - 5.3. Use Condition Failure Mechanisms
6. MEMS Device Trends
 - 6.1. Increased Functionality
 - 6.2. Spin-off Opportunities
 - 6.3. New MEMS Products
7. Conclusions

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek on-going just-in-time training that builds in-depth, advanced levels of MEMS technology and processing expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of MEMS technology.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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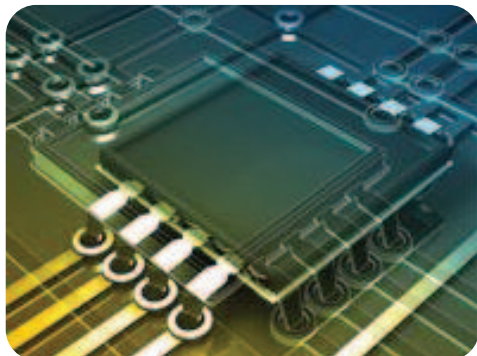
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**Semitracks will appear at the
International Reliability Physics Symposium
April 15 - 19
Anaheim, California**

Stop by and see us!



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Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

<http://www.semitracks.com>

*To post, read, or answer a question, visit our [forums](#).
We look forward to hearing from you!*

Upcoming Courses

(Click on each item for details)

Copper Wire Bonding

May 7 – 8, 2012 (Mon. – Tues.)
Munich, Germany

Failure and Yield Analysis

May 7 – 10, 2012 (Mon. – Thurs.)
Munich, Germany

Semiconductor Reliability

May 14 – 16, 2012 (Mon. – Wed.)
Munich, Germany

Polymers and FTIR

May 21 – 22, 2012 (Mon – Tues)
Penang, Malaysia

Polymers and FTIR

May 24 – 25, 2012 (Thurs – Fri)
Melaka, Malaysia

Wafer Fab Processing

June 5, 2012 (Tues)
San Jose, CA, USA

MEMS Technology

June 12 – 13, 2012 (Tues – Wed)
Enschede, Netherlands

Reliability Challenges

June 11, 2012 (Wed)
San Francisco, CA, USA

Copper Wire Bonding

July 11 – 12, 2012 (Mon. – Tues.)
San Francisco, CA USA