

InfoTracks

Semitracks Monthly Newsletter



Hybrid Microcircuit Packaging Part I

By Christopher Henderson

In this section, we'll provide an overview of hybrid microcircuit packaging. Although this technology may seem old to many viewers, hybrid microcircuits are still used extensively in military and space applications.

Popular in the 1970s and 1980s, hybrid microcircuits (Figure 1) are still common in many military applications. Hybrid microcircuits are composed of multiple technologies like resistors, capacitors, and integrated circuits. They have several distinct advantages for high reliability and extreme environments. They can be hermetically sealed to keep out moisture, and can be made using materials and

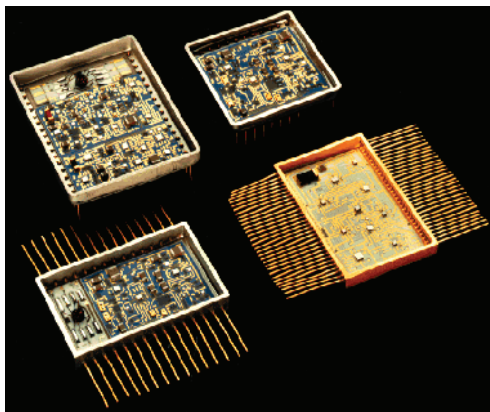


Image from Computer Desktop Encyclopedia

Figure 1. Hybrid microcircuits.

processes that permit operation over a wider temperature range than plastic encapsulated microcircuits. Hybrid microcircuits can be manufactured with thick film or thin film technology, and can be formed to create leads for surface mount or pins for through-hole mount.

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Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

Let's begin by looking at the materials used in thick film and thin film hybrid microcircuits (Figure 2). The elements of interest would be electrodes, a metal that makes contact to a non-metallic part of the hybrid, terminals that make contact to other metals, interconnect layers, resistors, and dielectric layers. There are thick film materials to do these functions as well as thin film materials. We'll begin with thick film materials.

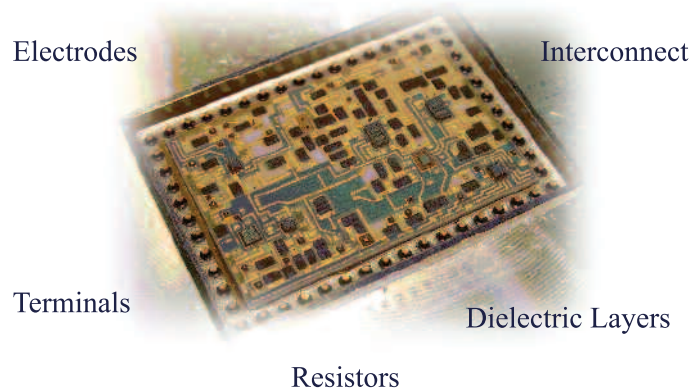


Figure 2. Thick/thin film packaging materials.

Thick film materials typically create layers greater than 25 microns thick. Silver and gold-based materials are common for conductors. Silver, silver-palladium, or silver-palladium-platinum pastes are used in a screening technology to create conductive traces on the substrate (Figure 3). These materials require an 850°C firing temperature to bond the material to the substrate. Gold-based materials are also common; however, the cost of gold is making this approach more expensive. Gold-platinum and gold-palladium-platinum are also quite expensive. The firing temperature is a few degrees higher than for that of silver. There are also some thick film dielectric materials. Many of these are proprietary, though.



Image courtesy Ferro Electronic Materials

Figure 3. Thick film packaging materials.

Thin film technology is manufactured differently than thick film technology hybrids (Figure 4). A thin film technology hybrid uses layers that are between 0.1 and 5 microns; therefore, the substrate must be extremely flat and uniform. This requires a fine-grained material like alumina, aluminum nitride or quartz. Sometimes they are polished to create a flatter, more uniform surface. The SEM image on the right shows an example of a small-grained, flat substrate. Thin film layers can be vacuum deposited through evaporation, or they can be sputtered. Numerous metals and metal alloys can be sputtered on a substrate. Some of the common ones are listed here. Metals can also be plated as well. Gold, nickel, and copper can be vacuum deposited or deposited through electroless deposition.

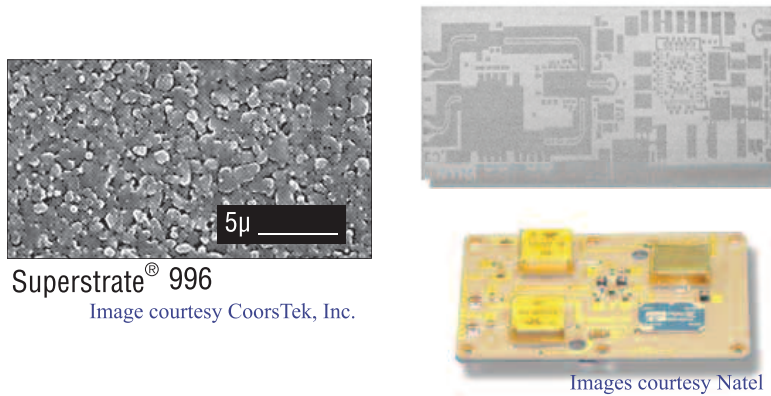


Figure 4. Thin film packaging materials.

There are three common substrate types: aluminum oxide or alumina, beryllium oxide, and aluminum nitride. Alumina is the most common substrate. It has a coefficient of thermal expansion that is relatively low, and it is inexpensive to manufacture. Figure 5 shows some of the common properties of alumina. Beryllium oxide has some nice properties—including a higher thermal conductivity—but beryllium is toxic. Therefore, special handling procedures are required. Many electronics manufacturers do not want to deal with the liability of beryllium, so it is not commonly used anymore. A substitute for beryllium oxide is aluminum nitride. It has a higher thermal conductivity, and better-matched coefficient of thermal expansion to silicon. As a result, it is receiving more attention.

Alumina content	Weight %	ASTM D2442	91	96
Color			Dark Brown	White
Bulk Density	g/cm ³	ASTM C373	3.72 min	3.75 min
Hardness - Rockwell	R45N	ASTM E18	78	82
Surface Finish	micro-inches Cutoff: 0.030 in; Stylus diameter 0.0004 in	Profilometer	≤ 45	≤ 35
Grain size (avg)	µm	Intercept method	5-7	5-7
Water absorption	%	ASTM C373	None	None
Flexural strength	kpsi	ASTM F394	53	58
Modulus of elasticity	Mpsi	ASTM C623	45	44
Poisson's ratio	---	ASTM C623	0.24	0.21
Coefficient of linear thermal expansion	25-200°C		6.4	6.3
	25-500°C		7.3	7.1
	25-800°C		8.0	7.6
	25-1000°C	ppm/°C	ASTM C372	8.4
Thermal conductivity	20°C 100°C 400°C	W/m-K	Various	13 12 8
Dielectric Strength (60 Hz AC)	0.025 in thick	V/mil	ASTM D116	540 600
Dielectric Constant @ 25°C	1kHz			11.8 9.5
	1MHz		ASTM D150	10.3 9.5
Dissipation factor @ 25°C	1kHz			0.1 0.0010
	1MHz		ASTM D150	0.005 0.0004
Loss Index @ 25°C	1kHz			1.2 0.009
	1MHz		ASTM D2520	0.05 0.004
Volume Resistivity	25°C			>10 ¹⁴
	300°C			4x10 ⁸
	500°C			---
	700°C	Ω-cm	ASTM D1829	4x10 ⁶

Figure 5. Alumina.

Let's move on and discuss resistors (Figure 6). Resistors are a common element within a hybrid microcircuit. They can be made using thick or thin film technologies. Lower resistance thick film resistors (a) are made of conductive metals, while higher resistance elements can be made from ruthenium oxide and other materials. These materials are typically deposited on alumina substrates. Thin film resistors (b) can be made from nickel alloys, nichrome, nichrome and tantalum pentoxide stacks, tantalum nitride, and other materials. The substrates are typically silicon dioxide or quartz. Thin film resistors can be made with top contacts for wirebonding, or with back contacts for better high frequency performance.

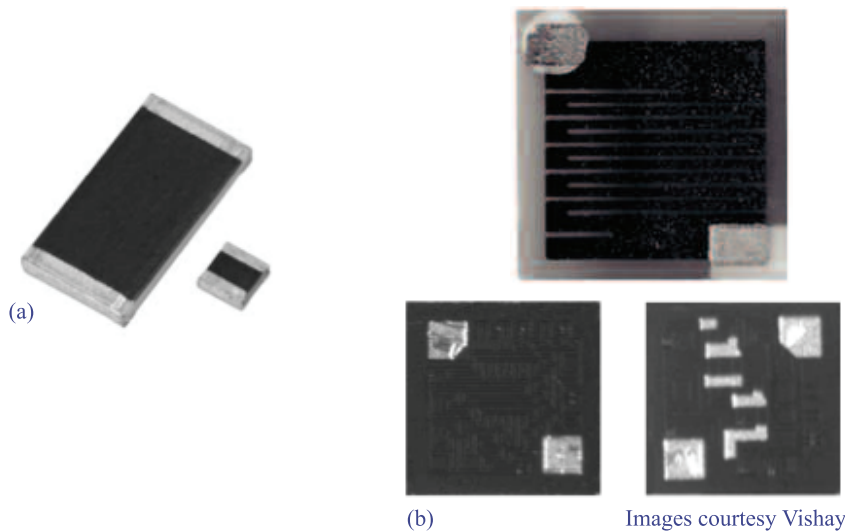


Figure 6. Thick/thin film resistors.

Capacitors are another common element in a hybrid microcircuit. Capacitors can also be made with thick and thin film technologies (Figure 7). Thick film capacitors (a) are typically made from ceramic or tantalum with electrodes at either end for connection, while thin film capacitors (b) are made using an aluminum-silicon dioxide-silicon, or MOS structure. They can also be made as metal-insulator-metal structures. Thin film capacitors are typically wirebonded.

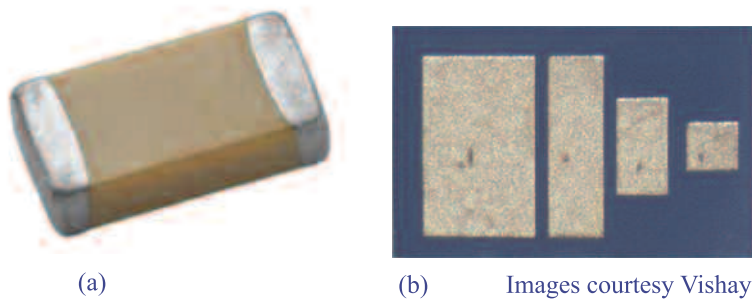


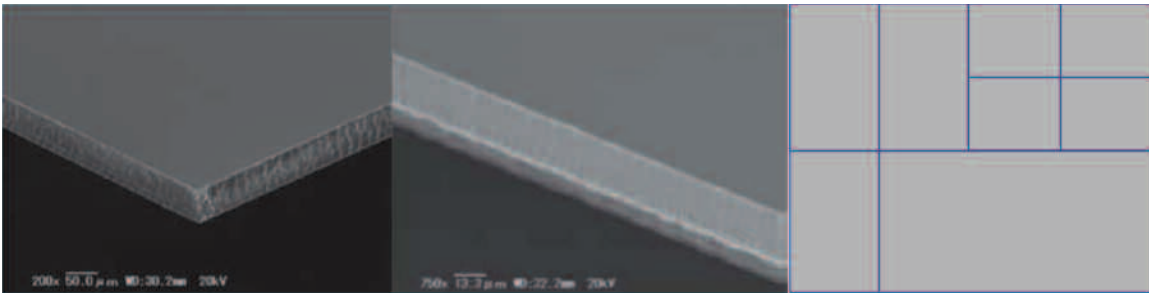
Figure 7. Thick/thin film capacitors.

Technical Tidbit

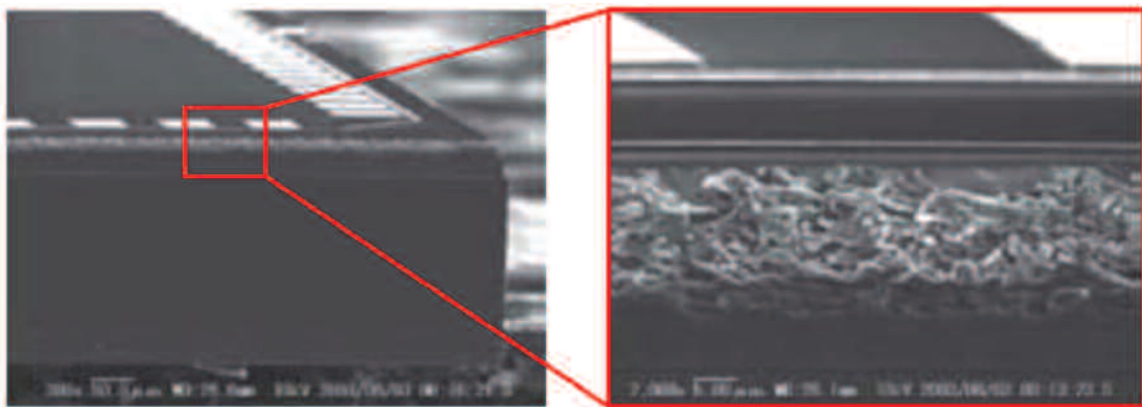
Laser Dicing

A newer method for singulation is the laser dicing method. Laser dicing uses a high-powered laser to either melt, cut, or initiate stress to facilitate singulation of individual dice.

There are three ways one can use lasers during the singulation, or dicing steps. The first is to use the laser in lieu of a traditional saw blade method. Here, the laser cuts through the entire silicon wafer. The second is to use the laser to create a groove, or trench, through the thin film layers and into the silicon to prevent delamination. The third is to use the laser to initiate a crack interface through the silicon, a technique referred to as stealth dicing.

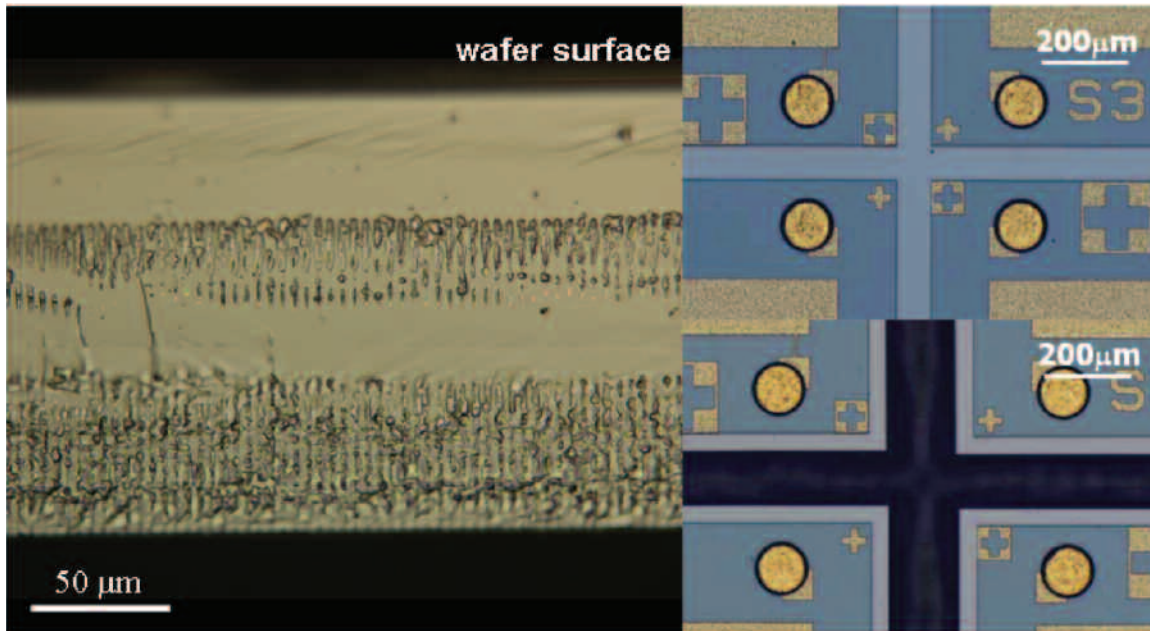


Delamination, or thin-film peeling, can be a problem with standard saw blade dicing when the chip uses low-k dielectrics. Laser grooving, which has no mechanical load, can be used to achieve high-quality processing with minimal delamination, thereby contributing to higher yield and improved reliability. The process is a two-step process. First, one uses the laser to cut a wide trench groove through the top thin films and into the silicon. This surface transforms into a melted edge through the low-k dielectrics, essentially sealing them to inhibit delamination. Second, one uses a thinner saw blade to cut through the remaining silicon in the middle of the groove.



Stealth dicing uses a 1064nm Nd:YAG laser to induce defects along the interface to be broken. The laser can initiate defects along interfaces at a rate of approximately 1 meter per second, so it is quite fast. Once the laser generates the defects, one can use the expansion of an adhesive material beneath the wafer to initiate cracking along the defect-laden interface, fracturing the wafer. Stealth dicing does not require cooling, and does not require a large kerf, leading to the potential for more product die per wafer. This

process also generates very little debris. One can also perform the stealth dicing step in conjunction with the laser groove step to minimize delamination problems with low-k dielectrics.



Laser initiated defects (Left), before adhesive material expansion (upper right), after adhesive material expansion (lower right)



Ask the Experts

Q: Package warping is becoming a big problem. Is there a JEDEC standard for package warping?

A: There are a couple of standards associated with package warping - JESD22-B112 and SPP-024A. JESD22-B112 was issued in 2005. However, this standard just discusses the techniques for measuring warpage. However, there is no general standard for what constitute an acceptable amount of warpage. For BGA device warpage, there is a JEDEC Standard Procedures and Practices document (SPP-024A) that is part of JEDEC Publication 95 (JEP-95). Tables 1 and 2 within the document give specifications in terms of ball pitch and ball height.

Spotlight: Semiconductor Reliability and Qualification

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. in particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability and Qualification*** is a four-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

What Will I Learn By Taking This Class?

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

Day 1 (Lecture Time 8 Hours)

1. Introduction to Reliability
 1. Basic Concepts
 2. Definitions
 3. Historical Information
2. Statistics and Distributions
 1. Basic Statistics
 2. Distributions (Normal, Lognormal, Exponent, Weibull)
 3. Which Distribution Should I Use?
 4. Acceleration
 5. Number of Failures

Day 2 (Lecture Time 8 Hours)

1. Overview of Die-Level Failure Mechanisms
 1. Time Dependent Dielectric Breakdown
 2. Hot Carrier Damage
 3. Negative Bias Temperature Instability
 4. Electromigration
 5. Stress Induced Voiding
2. Package Level Mechanisms
 1. Ionic Contamination
 2. Moisture/Corrosion
 1. Failure Mechanisms
 2. Models for Humidity
 3. Tj Considerations
 4. Static and Periodic stresses
 5. Exercises
 3. Thermo-Mechanical Stress
 1. Models
 2. Failure Mechanisms
 4. Interfacial Fatigue
 1. Low-K fracture
 5. Thermal Degradation/Oxidation

Day 3 (Lecture Time 8 Hours)

1. Package Attach (Solder) Reliability
 1. Creep/Sheer/Strain
 2. Lead-Free Issues

3. Electromigration/Thermomigration
4. MSL Testing
5. Exercises
2. TSV Reliability Overview
3. Board Level Reliability Mechanisms
 1. Interposer
 2. Substrate
4. Electrical Overstress/ESD
5. Test Structures and Test Equipment
6. Developing Screens, Stress Tests, and Life Tests
 1. Burn-In
 2. Life Testing
 3. HAST
 4. JEDEC-based Tests
 5. Exercises

Day 4 (Lecture Time 8 Hours)

1. Calculating Chip and System Level Reliability
2. Developing a Qualification Program
 1. Process
 2. Standards-Based Qualification
 3. Knowledge-Based Qualification
 4. MIL-STD Qualification
 5. JEDEC Documents (JESD47H, JESD94, JEP148)
 6. AEC-Q100 Qualification
 7. When do I deviate? How do I handle additional requirements?
 8. Exercises and Discussion

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

The Semitracks Analysis Instructional Videos™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.



International Symposium for Testing and Failure Analysis

**November 6-10, 2016
Fort Worth Convention Center
Fort Worth, TX, USA**

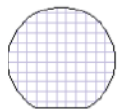
**Registration is available at
<http://www.asminternational.org/web/istfa-2016>**



Semitracks will be attending and will be available for meetings. Please contact us at info@semitracks.com to schedule a meeting.

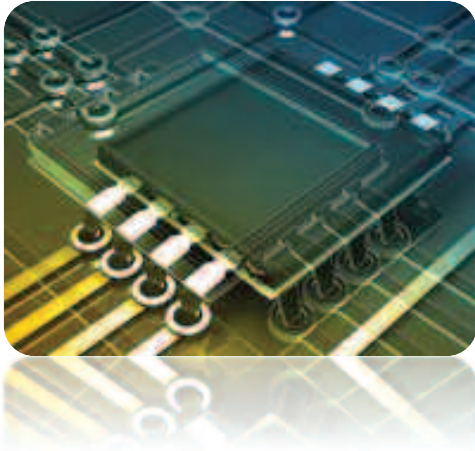
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Upcoming Courses

(Click on each item for details)

Semiconductor Reliability / Product Qualification

September 12 – 15, 2016 (Mon – Thur)
San Jose, California

Introduction to Processing

January 5 – 6, 2017 (Thur – Fri)
Shanghai, China

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