Issue 24 June 2011

InfoTracks

Semitracks Monthly Newsletter

Upcoming Webinar for EOS in Manufacturing

Although EOS and ESD damage can look quite similar to each other, the source of each and the solution can be quite different…

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Capacitance-Voltage Plotting

By Christopher Henderson

Capacitance-voltage or CV plotting, is a common electrical technique for investigating charge phenomena in MOS structures and transistors. In this article, we'll review some of the characteristics of the CV plot, and how it is used to identify and characterize yield and process integration problems.

Figure 1 shows a high and low-frequency capacitance-voltage plot of an ideal MOS structure. The solid line denotes the high frequency curve, while the dashed line denotes the low frequency curve. The capacitance is high when the structure is in accumulation, decreases toward the flatband condition at zero volts applied to the structure, and decreases further toward C_{min}, the steady state high frequency condition. In the low frequency condition, the capacitance begins to rise again at a voltage called the match point. As the voltage increases, the capacitance increases to a level similar to that in accumulation. This is sometimes referred to as a quasi-static CV measurement, and is measured using the voltage ramp method. In the voltage ramp method, the voltage is ramped very slowly at a given rate, typically less than 50 mV/sec. The measured displacement current is proportional to the capacitance. The frequency is considered to be low when the generation of electron-hole pairs keeps up with the signal. When the frequency is high, only majority carriers can follow the signal. At low frequencies, the charge exchange with the inversion minority carriers is in step with the varying signal. The small signal response dQ to dV appears at the surface (inversion) rather that at the depletion boundary. As the inversion layer forms, the capacitance increases back to $C_{max} \approx C_{ox}$.

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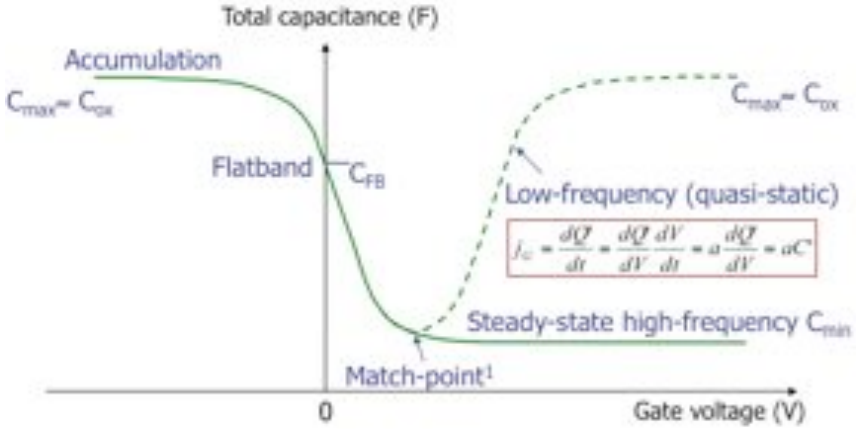
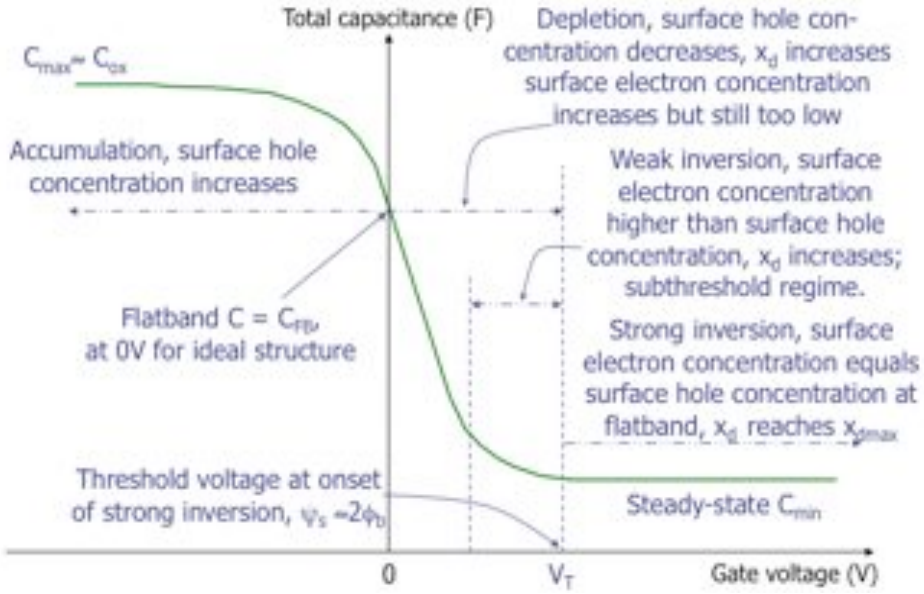


Fig. 1. High and Low Frequency Capacitance-Voltage plot of an ideal MOS structure.

Figure 2 shows a high-frequency capacitance-voltage, or CV plot of an ideal MOS structure. High frequency measurements allow the user to hide the effects of minority carriers since minority carriers cannot react fast enough to follow the signal. The capacitance is high, approximately that of the ideal capacitance across the oxide, when the voltage is negative. When the voltage is negative, the MOS structure is in accumulation, so the surface hole concentration increases, raising the capacitance. At flatband, the capacitance should be equal to the ideal capacitance for the flatband condition. As the voltage goes positive, the MOS structure goes into depletion. The surface electron concentration increases, but remains at a level too low to offset the decrease in surface hole concentration. In weak inversion, the surface electron hole concentration is higher than the surface hole concentration, but the depletion width increases, lowering the capacitance further. In strong inversion, the surface electron concentration equals the surface hole concentration at flatband, and the depletion width reaches its maximum. The capacitance reaches it's minimum at this value as well. This is also the threshold voltage point, where ψ_s is approximately equal to $2\phi_b$. The steady-state condition is reached when sufficient electrons are supplied to the surface mechanisms like electron-hole pair generation.



*****The conclusion of this article will be delivered next month!*****

Ask the Experts

Q: How can I limit the breakdown damage when an oxide is stressed in a Power MOSFET device?

A: Use a current limiting resistor or set a lower compliance limit on the SMU. A more active monitoring circuit may be needed if the FN tunneling current is already significant.

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

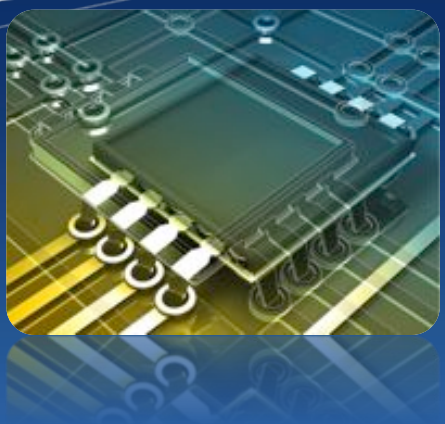
AMFA 2011

ADVANCED MATERIALS & FAILURE ANALYSIS

August 29, 2011
Boston, Massachusetts

The 6th Annual AMFA is just around the corner! Please plan now to attend; registrations are open until July 30th. Semitracks' President Christopher Henderson will be running the event this year.

Learn more about this conference at:
http://www.amfaworkshop.org/



EOS in Manufacturing Webinar

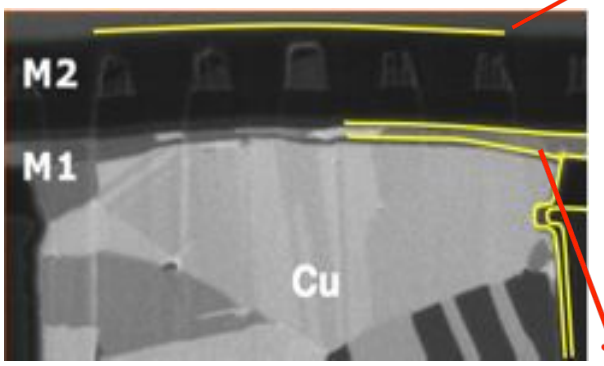
Electrical Overstress (EOS) and Electrostatic Discharge (ESD) account for most of the electrical failures of devices that occur in factories and in the field.. The effects of ESD on integrated circuits have received much attention in technical literature, standards bodies and educational workshops and tutorials. The problem has been approached in a systematic manner which has resulted in relatively successful practices for design of robust devices and control procedures for the factory. However, the same cannot be said for the effects of the broader categories of electrical stresses generally referred to as electrical overstress (EOS). This disparity is reflected in the typical Pareto analysis of failures in electrical assembly where EOS is often the most commonly assigned cause of failure and may exceed the incidence of ESD by 10 times or more. One of the main reasons for this is that EOS sources are widely varied and very application dependent. As a result, no simple broad models for EOS have emerged comparable to HBM and CDM for ESD. Common device design practices have not been developed to the same extent, system level approaches tend to be ad hoc and responsibility for controlling potential sources in manufacturing tends to be diffused or non-existent.

Learn more at:
http://www.semitracks.com/index.php/en/courses/public-courses/analysis/eos-in-manufacturing

Technical Tidbit

There is currently a lot of research and development work on Through-Silicon Vias or TSVs. Although polysilicon in the TSV makes for a good material from the standpoint of a good thermal match, manufacturers would prefer to use copper, since it has a much lower resistance. Copper has a much higher coefficient of thermal expansion than silicon, leading to several failure mechanisms. A common failure mechanism is a phenomenon called copper pumping. During thermal cycling, the copper expands and contracts, alternately pressing up on the back end of the line (BEOL) materials, and relaxing back. This creates the bulge seen in this image. This pumping action causes stress in the BEOL layers, leading to BEOL damage, or cracking in the metal and dielectric layers. Most process engineers work to reduce the copper pumping effect through the use of annealing and sintering. These steps increase grain size and reduce the coefficient of thermal expansion somewhat.

TSV and BEOL bulging after device sintering



Metal 1 thinner on TSV due to bulging

Upcoming Courses

EOS in Manufacturing

June 28th, 2011 – Webinar

ESD Design and Technology

July 10-12, 2011 – Tel Aviv, Israel

ESD Design and Technology

August 23-25, 2011 – San Jose CA

IC Packing Metallurgy

September 12-13, 2011 – Munich, Germany

Water Fab Processing

September 26-29, 2011 - Singapore

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or e-mail us at info@semitracks.com.

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by email at jeremy.henderson@semitracks.com.

We are always looking for ways to enhance our courses and educational materials.

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