Issue 17 November 2010

InfoTracks

Semitracks Monthly Newsletter

Visit Semitracks at ISTFA

The International Symposium for Test and Failure Analysis (ISTFA) will be held November 14-18 at the Intercontinental Hotel in Dallas Texas. Semitracks will be exhibiting at the conference, please stop by and see us at booth 217.

Read more, Page 3

Training: The Need is Becoming Critical – Part 2

By Christopher Henderson

Analysis – The Current Situation

Today's analyst faces a much different situation than the analyst of the late 1960's. While we still have standard digital logic circuits like the quad, two-input NAND gate, we also have integrated circuits that exceed 10 million gates. In addition the bipolar silicon circuits of the late 1960's, we have a bewildering array of technologies, such as complementary metal oxide semiconductor (CMOS) circuits, BiCMOS circuits, gallium arsenide circuits, indium phosphide circuits, silicon carbide transistors, gallium nitride diodes, complex heterojunction structures, and microelectromechanical systems (MEMS). We also have a variety of design complexities, including discrete components, digital circuits, analog circuits, memory circuits, MEMS devices, radio frequency and optoelectronic components. An example of the circuits analysts now face is shown in Fig. 2.

Today's analyst also faces more complex equipment sets. In addition to the curve tracer, optical microscope and decapsulation tools, the analyst must be familiar with a variety of electrical testing hardware, endless electrical fixture configurations, x-ray and acoustic microscopy, electron beam tools, optical beam tools, thermal detection techniques, the focused ion beam (FIB), the scanning probe/atomic force microscope, and a bevy of surface science tools. Many times, the analyst must make do with a limited set of tools, as the cost of purchasing these tools exceeds the budget of all but the most lavishly funded operations.

Continued on Page 2

In this Issue:

Pages 1 & 2	Training: The Need is Becoming Critical – Part 2
Page 3	Ask the Experts: Cumulative Probability
Page 3	Announcements: ISTFA 2010
Page 3	Course Spotlight: Catalyte IC Exclusive
Page 4	Looking Ahead: List of Upcoming Courses 2011
Page 4	Upcoming Courses

(continued)

Today's analyst also faces enormous pressures from the customer. The customer wants an answer to the problem immediately. Even so, there may be little, if any, ability to impact the manufacturing process. Because product cycle times are so short, many components are manufactured with a few wafer runs and are not manufactured again. The analyst's company may not even manufacture the device; it may be sent to a foundry for fabrication. The analyst may be doing activities other than analyzing field return failures. He or she may be performing design debug, yield improvement, or qualification analysis.

Today's analyst must know a staggering amount of information and be able to lucidly process that information to successfully guide an analysis through to completion. While the analyst of the late 1960's could get by with a basic understanding of design, test, packaging, and some analysis tools and techniques, today's analyst must know a whole lot more. We are expected to understand the correlation between the design and layout of multi-million transistor circuits, even though the design engineers can't perform that task (all they know anymore is VHSIC Hardware Description Language (VHDL), Register Transfer Language (RTL), and other abstraction languages). We are expected to understand how to test complex integrated circuits, even though the test engineering community cannot figure out how to adequately test these devices. We are expected to have non-destructive depackaging techniques available for an ever-increasing number of package configurations, even though the packaging engineers cannot successfully rework these configurations. We have to understand obscure properties like the Franz-Keldyish effect, the Seebeck effect, and escape peaks.

The task of performing failure analysis is daunting. Over a career, an analyst is likely to experience many of these issues listed above. Education and training play an important role if the analyst is to be successful in his or her work. How do we prepare analysts for this environment? Please read next month's issue to see the approach to succeed in this seemingly impossible environment.

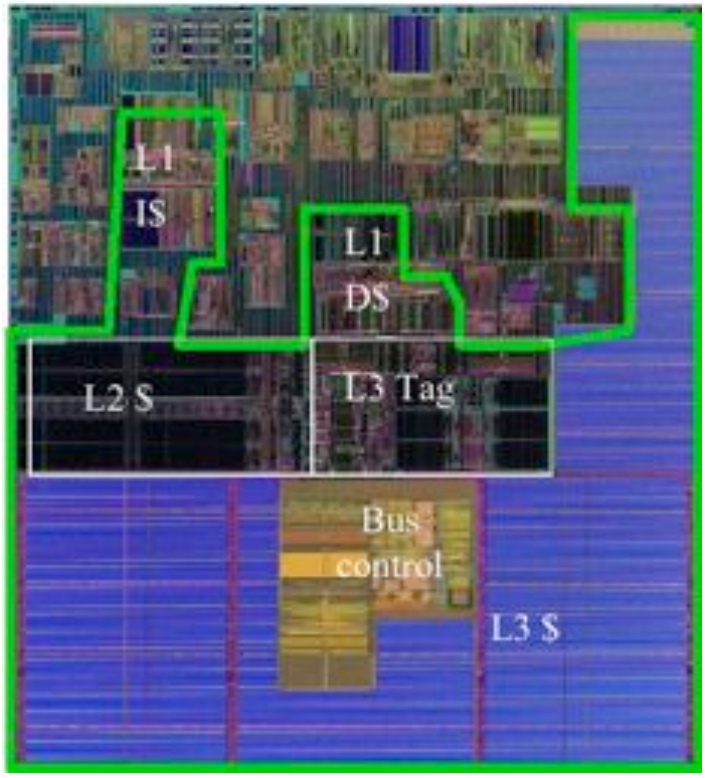

Fig. 2. Photograph showing the Intel Itanium™ processor containing in excess of 1 billion transistors (photo courtesy Intel).

Ask the Experts

Q: Sometimes I see i/(n+0.5) used for median ranks, and other times I see (i-0.3)/(n+0.4) used for cumulative probability in probability plots. Is one better than the other?

A: The second formula (i-0.3)/(n+0.4) is the more accurate approach. If you scale down to a sample size of 1, it correctly resolves to 0.5 for a cumulative probability. i/(n+0.5) resolves to 0.66, which is not as accurate. If you are doing calculations by hand, then i/(n+0.5) is quicker, but since most people will use a program like Excel or Relex to do these calculations, it is better to use (i-0.3)/(n+0.4).

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Looking Ahead

List of Upcoming Courses 2011

ESD Design and Technology
December 14-16, 2010 – Malaysia

Failure Analysis
January 18-21, 2011 – Malaysia

Semiconductor Reliability
January 24-27, 2011 – Malaysia

IC Packaging Metallurgy
January 24-25, 2011 – San Jose

Defect Based Testing
January 2011 – Ireland

Semiconductor Packaging Design, Simulation, and Technology
January 30-Febuary 2, 2011 – Tel Aviv

Interconnect Process Integration
February 3, 2011 – San Jose

Continued on Page 4

Announcements: ISTFA 2010

November 14-18, 2010
InterContinental Hotel
Dallas, TX, USA

Stop by and see us at booth 217

Enrich your career at the 36th International Symposium for Testing and Failure Analysis, November 14-18 in Dallas, Texas. Acquire the latest knowledge from the field's leading professionals with six days of tutorials, short courses, technical presentations, panels, and user groups. Research leading edge instruments and solutions at the industry's largest dedicated equipment expo. Meet and network with hundreds of your peers from novice to expert. Find out more about ISTFA 2010.

Semitracks is proud to partner with Catalyte IC to provide the following courses to our members:

SoC Power Management Design and Verification – Dr. Bhanu Kapoor, President, Mimasic
Design and Verification with SystemC – Dr. Bhanu Kapoor, President, Mimasic
IC ESD protection – Design, optimization and qualification –
Dr. Vesselin Vassilev, Director of Technology, Novorell
Custom Design Flow – Basic to Advanced – Faizul Alam, CTO, CatalyteIC
Designing an IC – Concepts through Implementations – Faizul Alam, CTO, CatalyteIC
Introduction to system verilog for designers and verification engineers –
Paul Hylander, CEO, HyperAnalytix
Fundamentals of RF and Wireless Performance Testing –
Dr. Claudio Montiel, Asst. Professor, Texas A & M
DFT Beyond Scan – Dr. Robert Molyneaux, President, ChipBridge
Design and Productization of Digitally – Intensive RF Transceiver SoCs – Dr. Oren Eliezer CTO, Xtendwav

Learn more at: http://www.catalyteic.com/training

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Semiconductor Reliability
February 16-18, 2011 – San Jose

Failure Analysis
February 28-March 3, 2011 – San Jose

Analog Mixed Signal Product Engineering
February 21-24, 2011 – Ipoh

Wafer Fab Processing
February 2011 – San Jose

Wafer Fab Processing
February 2011 – Malaysia

Yield Analysis
March 10-11, 2011 – Malaysia

IC Packaging Design & Modeling
April 18-20, 2011 – Malaysia

SSL LED
April 21-22, 2011 – Taiwan/Malaysia

Introduction to Biotechnology
May 2011 – Austin

Reliability Characterization & Challenges
May 9-10, 2011 – Malaysia

Interconnect Process Integration
June 13-14, 2011 – Malaysia

Semiconductor Technology
August 11-12, 2011 – Malaysia

Advanced Thermal Management
September 7-9, 2011 – Malaysia

Upcoming Courses

ESD Design and Technology
December 14-16, 2010
Kuala Lumpur, Malaysia

Failure and Yield Analysis
January 18-21, 2011
Kuala Lumpur, Malaysia

IC Packaging Metallurgy
January 24-25, 2011
San Jose, CA, USA

Defect-Based Testing
January 2011
Ireland

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or e-mail us at info@semitracks.com.

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by email at jeremy.henderson@semitracks.com.

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our website!

http://www.semitracks.com