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SEMITRACKS
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NEWSLETTER

INFOTRACKS

Upcoming Courses

Semitracks offers live seminars in Europe, North America, and Asia, and our online classes can be accessed anywhere in the world. Click on any course title to find out more.

Failure and Yield Analysis
September 8-11, 2009
Munich, Germany

Semiconductor Reliability
September 14-16, 2009
Munich, Germany

MEMS Technology
October 5-6, 2009
Austin, TX, USA

Photovoltaics Overview
October 7, 2009
Austin, TX, USA

Photovoltaics Technology and Manufacturing
October 8, 2009
Austin, TX, USA

Wafer Fab Processing
October 19-22, 2009
Enschede, Netherlands

Photovoltaics Technology and Manufacturing
October 30, 2009
Anaheim, CA, USA

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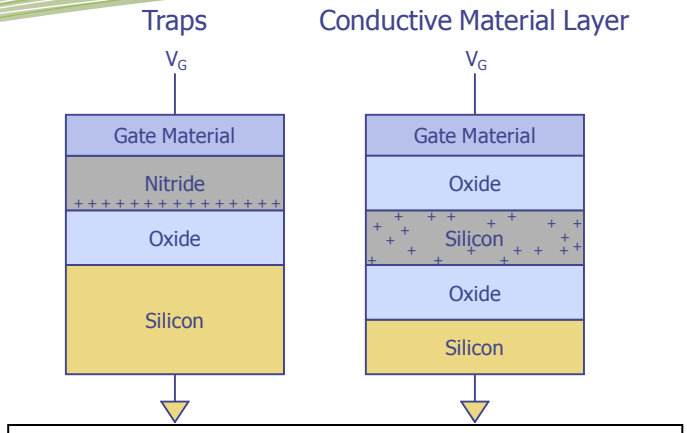
For information about online courses, click here.



MNOS (left) and FAMOS (right) non-volatile memory structures.

[inside this issue]

A Brief History of Non-Volatile Memory

[By Chris Henderson]

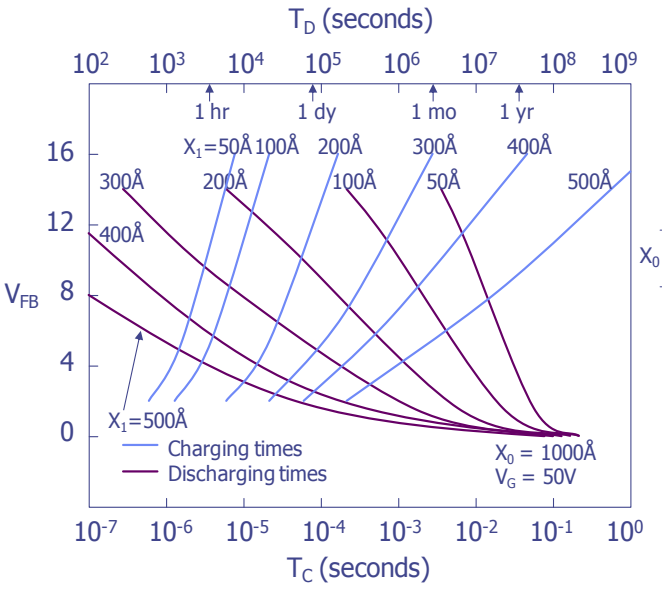
Part 1

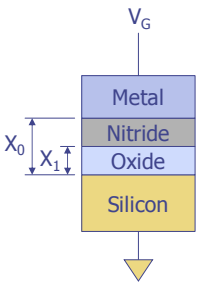
Non-volatile memory, which can hold data with power removed, has become critical to devices like PDAs, cell phones, and digital cameras. Over the next several issues, this three-part article series will discuss basic non-volatile memory technologies to give you a better understanding of their background and importance.

In Part 1, we will cover one of the original non-volatile memory technologies, the metal nitride oxide silicon, or MNOS technology. Part 2 will discuss an improvement over MNOS called silicon oxide nitride oxide silicon (SONOS) technology, and its predecessor, silicon nitride oxide silicon (SNOS). Next, we'll discuss the floating gate avalanche injection MOS or FAMOS transistor, used extensively for years in ultraviolet erasable memory. One of the more popular variants of this technology is flash memory. Part 3 will cover the strengths and weaknesses of NAND and NOR, the two most common non-volatile memories in use today.

Two basic mechanisms store charge in non-volatile memory. The first method, which forms the basis for MNOS technology, utilizes traps in the insulator or at an interface. The second method, called floating gate technology, stores the charge on a conductive or insulator material sandwiched in between the control gate and the silicon channel.

In 1967, Richard Wegener and his colleagues at the Sperry Rand Research Center developed the metal nitride oxide silicon transistor (MNOS) while researching technologies to help store data and reduce power dissipation in military electronics. When they replaced the oxide layer in a standard MOS transistor with a nitride-oxide stacked layer, the bonds between the nitride and the oxide created an interface containing a high level of traps (unterminated bonds that attract positive or negative charge). Placing a high voltage on the gate forced charge onto these interface traps, while placing a high voltage of the opposite polarity on the gate removed the interface traps. One disadvantage of this technique is that trapped charge tends to disperse or recombine, limiting the storage time of the structure. The higher the storage temperature, the more quickly the charge recombines. Researchers have been able to improve the retention time by replacing the top metal gate with a silicon gate.





The figure on the left illustrates the basic MNOS cell structure and a graph of the structure's charging and discharging times. The graph shows an example set of curves for a combined dielectric stack of 1000 angstroms and differing oxide thicknesses. For thinner oxides, the charging and discharging times decrease substantially. However, a MNOS structure requires a long charging time to retain trapped charge. Conversely, a short charging time leads to a short discharge time. Because of this problem, MNOS memory never became popular as a high-volume commercial technology. However, its greater tolerance of radiation made the MNOS suited for some niche applications, such as military and space.

Don't miss these upcoming conferences!

ESREF 2009

October 5-9
Bordeaux, France

The 20th International Symposium on Reliability of Electron Devices will focus on recent developments in quality and reliability management of materials, devices and circuits for micro-, nano-, and optoelectronics. For more information, visit the website.

ISTFA 2009

November 15-19
San Jose, CA

The 35th International Symposium for Testing and Failure Analysis is your opportunity to hear original, unpublished work on FA topics presented by industry professionals. For more information, visit the website.

Technical Tidbit

[Wafer Level Bake]

Wafer level bakes have gained in importance in recent years for several reasons. Like wafer level testing, wafer level bakes can be performed prior to packaging, allowing engineers to send results to process engineers more rapidly. Wafer level bakes are primarily used to study temperature-only driven mechanisms, charge retention in non-volatile memories, and mechanisms like gate sinking in pHEMTs (High Electron Mobility Transistors). Another advantage of the wafer level bake is that one can stress components at higher temperatures than normally possible in packaged devices. Wafer level bakes are typically performed at 250-275°C. This is particularly useful for memory retention tests, since most devices are specified to work for 10 years or longer. A higher temperature stress allows the engineer to compress the stress test into a shorter time period.

Burn-in system (photo courtesy Tandex Labs)

Wafer level bakes have been used for some time. They started in the mid-1980s as engineers began to study charge retention in EEPROMs. David Baglee et. al. mention wafer level bakes in their 1990 paper on EPROM reliability.[1] Prior to this, many engineers performed bakes on packaged components to study this problem as well as other oxide reliability problems. Wafer level bakes are not typically used for standard reliability testing on logic devices, since the better model for thicker oxides (>50Å) is the Eyring model (a model that includes both voltage and temperature), or the Power Law model (a model that is sometimes used for ultra-thin oxides, or those less than 50Å).

[1] David A. Baglee, Lynn Nannemann, and Cheng Huang, "Building Reliability into EPROMs," Proc. Int. Reliab. Phys. Symp., 1990, pp. 12-18.

Customer Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please feel free to call us at 1-505-858-0454 or e-mail us at info@semitracks.com.

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the October newsletter, please contact Alicia Constant by email at alicia.constant@semitracks.com.

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our website! www.semitracks.com

Course Spotlight

[Photovoltaics Overview]

You've seen the headlines: "Global Energy Demand Expected to Soar by 2030." "Escalating Oil Prices Threaten Economic Recovery." According to the US Department of Energy, the demand for energy in the United States alone will swell by 32% by the year 2020, [1] and the Energy Information Administration projects a 44% increase in world oil consumption by 2030.[2] Solar power—the clean, renewable energy source of the future—is becoming more and more crucial to our economic and environmental welfare.

Since the 1970s, stunning breakthroughs in photovoltaic technology have made clean, light-generated electricity more feasible and economical. As many companies rapidly introduce new technologies to harness solar power, tracking developments—let alone understanding them—can be daunting. Semitracks' Photovoltaics Overview course analyzes and distills the most important aspects of this complex technology. This course is necessary for every manager, engineer, and technician entering the photovoltaic field, whether they are working directly for a photovoltaic manufacturer or system integrator or selling to PV manufacturers.

In ***Photovoltaics Overview***, participants learn the basics of photovoltaic technology, the steps involved to integrate PV modules, and methods to address the issues that arise.

The course covers five major topic areas:

1. Background Information. Participants learn about the history of solar technology, recent declines in PV costs, solar resources on the planet, and current applications of solar photovoltaics.
2. Energy Economics. Photovoltaics will only become widespread when the cost can compete with other energy technologies. Participants learn to calculate capacity factors, capital costs, energy demands, peak usage, and storage methods.
3. Types of PV. The course covers monocrystalline silicon, polycrystalline silicon, silicon thin film technologies, compound semiconductor technologies, and multi-junction cells.
4. Module Construction. Attendees learn about cell classification, interconnect technology, and testing. They will also study laminate assembly technologies, including the glass polymers, the resin/glass sandwich construction, and the backplane. We will spend time discussing the durability, safety, and transmission properties of the top glass. Participants will also learn the costs and trade-offs in module manufacturing.
5. Photovoltaic Systems. Participants will learn about the power output and costs and understand the effects of latitude and climate. They will also be introduced to tracking systems and calculate the tradeoffs associated with tracking, shading, and other effects.

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To find out more about our other courses, click here.

Questions & Answers

Q: *Where can I find some current papers on NTBI? -Joey*

A: Joey, the best place to find information on the NBTI mechanism is in the Proceedings of the International Reliability Physics Symposium. The most important papers can be found in the last 6-7 years of proceedings, as it has become a major issue in recent years. We also have a good summary with reference to key papers in our Online Training system, http://semitracks.com/index.php/en/online-training, if you're interested. Best regards, Chris

To post, read, or answer a question, visit http://www.forums.semitracks.com. We have recently updated our forums! Even if you have previously registered, you will need to reregister in order to post. We look forward to hearing from you!