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this issue:

Soft ESD Failures

[By Chris Henderson]

This article is the first in a two-part series on recoverable failures related to package charging. Sometimes, these failures are referred to as soft electrostatic discharge (ESD) failures. In a soft ESD failure, components with an electrically verified failure unexpectedly recover during the course of the analysis. Recovery can happen during an electrical retest after decapsulation, an electrical retest after bake, or an electrical retest after x-ray.

Soft ESD failures can be frustrating to identify. Some of their common attributes include the following:

- High fallout rates at printed circuit board assembly.
- Burn-in-induced failure in some high voltage plastic-packaged components.
- An electrical signature indicating an elevated power down current, standby current, or quiescent power supply current (IDDQ).
- Leakage on some I/O pins, indicating transistor channel leakage.
- Hard ESD failures occurring with soft ESD failures.
- Partial or complete component recovery after decapsulation.
- Recovery of hermetic package after x-ray radiography but not after bake.
- Recovery of plastic packages after both bake and x-ray.
- Recovery of plastic packages after removal of the component from the printed circuit board.

Soft ESD failure mechanisms have been observed in both hermetic and plastic packages. In hermetic packages, the die is packaged inside a cavity with an inert environment, typically a low humidity nitrogen gas. The package construction uses ceramic or metal and prevents moisture and contamination from entering the cavity.

Plastic packages are non-hermetic. Over time, moisture and contamination can penetrate the epoxy thermoset to reach the surface of the die. Failure analysts have observed soft ESD mechanisms attributable to freeze spray and sandblasting in hermetic packages and component handlers in plastic packages.

Three significant conditions can cause soft

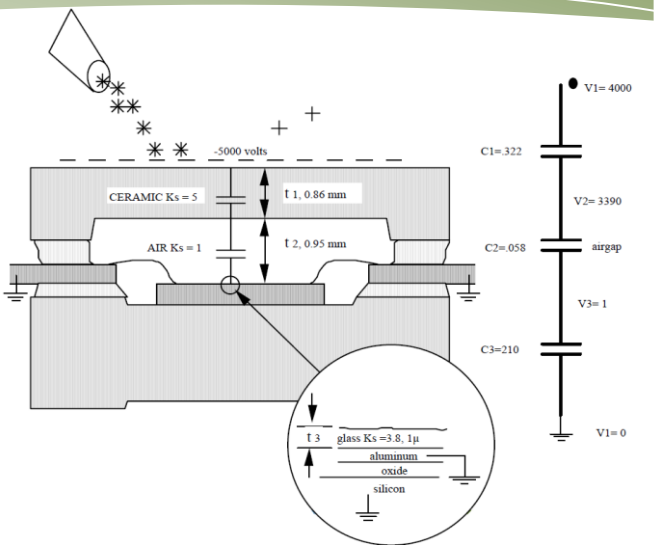


Figure 1: Failure model for soft ESD in a hermetic package.

ESD failures in hermetic components. At the International Reliability Physics Symposium in 1978, Murray Woods and Gary Gear published work on the role of freeze spray application in soft ESD failures. Additionally, in the early 1980s, engineers at Signetics documented problems with the sandblast process and the use of ungrounded rails in IC handlers.

Figure 1 illustrates the failure model for soft ESD in a hermetic package. Freeze spray, sandblasting, or an IC sliding down the handler plastic tube introduces a significant charge onto the surface of the package. The insulating materials can in turn lead to a high voltage, sometimes in the thousands of volts. The electrical properties of the package, hermetic air gap, and IC materials all affect the final voltage at the IC level. Capacitance is a function of the dielectric constant of the material, the area of the material, and its thickness. In Fig. 1, the specific capacitances of the ceramic, air gap, and top glassivation layer on the IC lead to a given voltage on the IC.

In a simplified model, the hermetic package and die can be represented by three capacitors in series. Basic electronics theory teaches us that voltage divides according to 1/C. The passivation layer has the largest capacitance and is essentially ground. The lid has a higher dielectric constant and, therefore, a larger capacitance. Because less voltage drop occurs across the ceramic lid than across the air gap, the largest voltage drop occurs across the cavity. Now, the cavity ambient environment is at a reduced atmospheric pressure. The breakdown

voltage is approximately 15 kV/cm in an air environment. Since the air gap is only about 1mm, a corona discharge can occur in the cavity. The negative charge associated with the discharge event drifts to the most positive potential: the bond wires and the passivation layer.

The table in Figure 3 shows capacitance per unit area, dielectric constant, thickness and breakdown voltages for the air gap, glassivation layer, and ceramic lid materials. The table uses the electrostatic unit of charge (esu), also called the statcoulomb. All the other esu units are defined in terms of the esu unit of charge and the centimeter, gram, and second.

Figure 4 illustrates the electrical charge influence on a transistor in a junction isolated IC. At the beginning of the process (see left-hand image), the top of the ceramic lid charges negative. The ceramic and air gap initially stand off the high voltage. However, as the voltage on the ceramic lid increases, the voltage across the air gap exceeds the breakdown voltage, resulting in a corona discharge. After the discharge, a negative charge occurs on the top of the glassivation layer (see center image). The charge on the glassivation layer inverts the lightly doped n-epitaxial layer below the surface, resulting in leakage or, in severe cases, functional failure. When a positive charge is applied to the lid of the ceramic (see right-hand image), the epitaxial layer is not inverted. However, if the epitaxial layer is inverted, the positive charge can cause IC recovery.

In 1978, scientists at Intel discovered that certain Electrically Programmable Read Only Memories (EPROMs) would fail when subjected to freeze spray. Freeze spray is sometimes used to cool devices individually on an ad-hoc basis. After a lengthy analysis, they traced the problem to charge buildup on the lid. The charge was placed on the lid by friction created when solid carbon dioxide particles impacted the ceramic lid. The charge broke down the air gap within the package and deposited charge on the surface of the die, affecting memory cells. Additionally, deposited charge on the die surface created an N inversion layer in the structure, resulting in leakage.

The Intel scientists discovered that EPROM devices recover when illuminated with ultraviolet light through the programming window. Furthermore, they discovered that ultraviolet light is effective when the energy is greater than 4.3 electron volts. They also discovered that devices recover when they are decapped and the die is rinsed in water or isopropyl alcohol. Figure 7 shows the silicon-silicon dioxide band diagram for the basic structure. If the ultraviolet light energy is greater than 4.3 electron volts, it can raise the energies of the carriers to the point where they can overcome the barrier

In 1983, engineers at Signetics discovered a similar charging problem with sandblasting operations. In this case, Signetics engineers grounded the components in socketed boards to prevent electrostatic discharge. Although some failures still occurred, they manifested themselves differently than typical ESD failures. The failures showed 500 ohm shorts between the supply voltage and ground. After partial recovery, the leakage curve exhibited a parabolic shape, indicative of transistor channel leakage. When delidded, the short on the components recovered. When the lid was cracked, exposing it to air more slowly, the short slowly recovered. The engineers noticed that the short did not recover when delidded in a dry nitrogen environment, leading to the conclusion that moisture in the air helped the shorts to recover. Engineers also noticed that the shorts did not recover with a 150 degree centigrade bake, but would recover when x-rayed for 3 minutes at 70kV accelerating voltages in the x-ray system.

	Capacitance/Unit Area	Dielectric Constant (K_s)	Thickness (t)	Breakdown Voltage
Air gap	0.058	~ 1.0	0.950 mm	~ 30 kV/cm STP ~ 15 kV/cm at 0.5 atm
Glassivation	210.0	~ 3.8	0.001 mm	> 7 MV/cm
Ceramic	0.322	~5.0	0.860 mm	> 1MV/cm

$C/A=K_sE_0/t$ (esu/v-μm^2), where E_0=55.4 (esu/v-μm)

Figure 3: Table relating capacitance per unit area, dielectric constant, thickness and breakdown voltages for the air gap, glassivation layer, and ceramic lid materials.

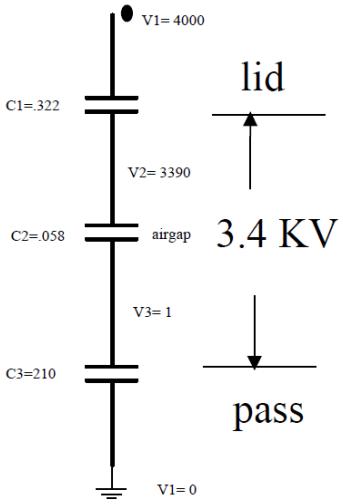
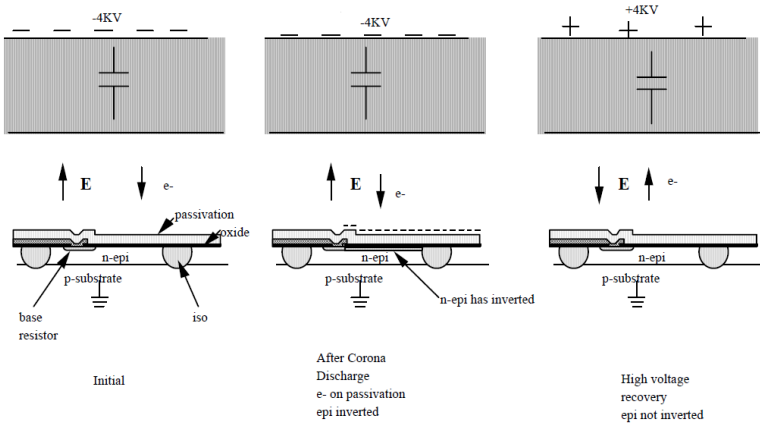


Figure 2: The hermetic package and die are similar to three capacitors in a series.



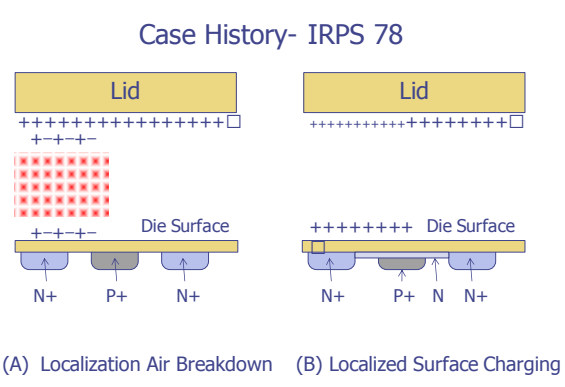


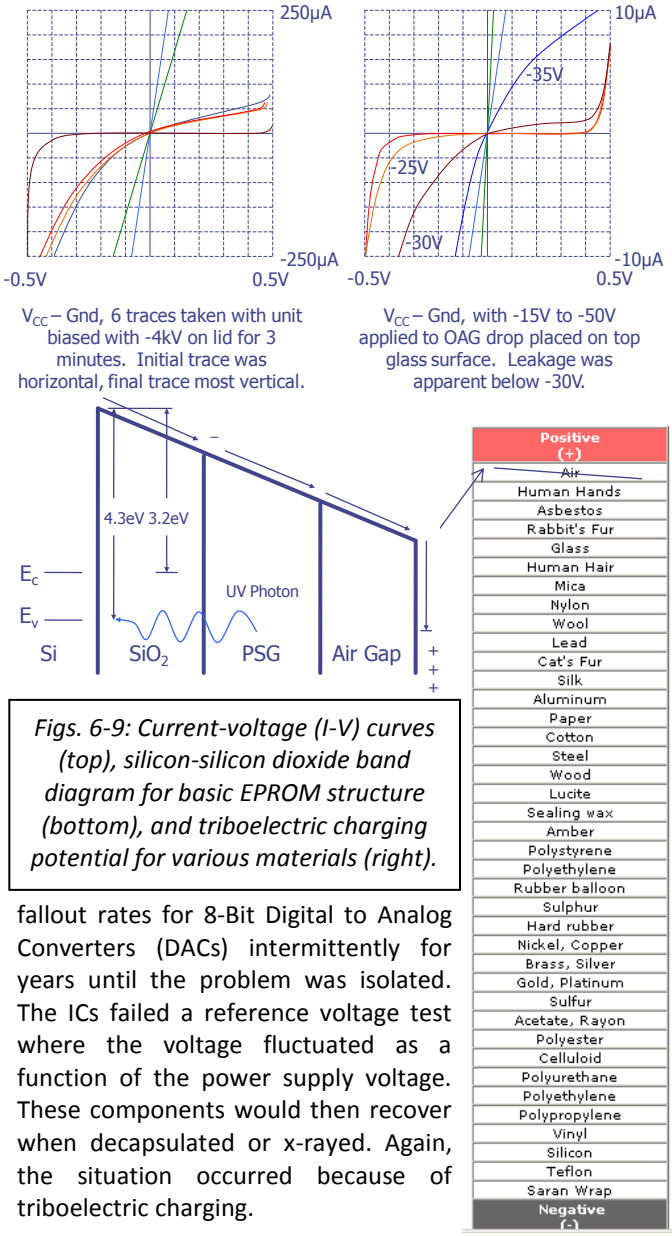
Figure 4 (top): Electric charge influence on a transistor in a junction isolated IC. Figure 5 (left): EPROMs reacting to freeze spray.

The engineers then attempted to replicate the failures. They found they could replicate the symptoms by using a probe to place -100 volts on the top of the glassivation layer. They could also replicate the problem by applying a large negative voltage to the lid of the component. The failure recovered when they placed a large positive voltage on the lid of the component. Finally, they reproduced the failure symptom using a ZeroStat charge gun on the lid of the component.

The two sets of current-voltage (I-V) curves opposite illustrate the leakage. The curves on the left indicate increasing leakage when -4kV is placed on the lid of the component. The curves on the right show increasing leakage when varying voltages are applied to a droplet of insulating material on top of the glassivation. Leakage becomes apparent when the voltage is less than -25V.

Historically, many scientists assumed air friction caused positive triboelectric charging. The table on the far right indicates the triboelectric charging potential for a variety of materials. Scientists like Baumgartner postulated that air may be misclassified. Tests made by flowing air over a range of surfaces found very little voltage buildup. Some hot air sources were found to be charge generators, possibly due to the nature and temperature of the heating element. Hot plastic was found to be particularly susceptible to triboelectric charging. Positive elements give up electrons, but in air, the dust may be a factor. Large amounts of dust are generated during the sandblasting process. The heating coil material may also be a factor. For more information, see G. Baumgartner "The Misconceptions of Air Flow as A Tribocharging Source," EOS/ESD Symposium, 1992, 1.2.1.

A third well-documented incident involving recoverable failures due to charging was publicized in the late 1980s by Signetics. In this case, Ceramic Dual Inline Packages (CERDIPs) were loaded into an IC handler with ungrounded rails. The rails were improperly grounded because of a missing ESD kit. Signetics experienced high fallout rates for 8-Bit Digital to Analog Converters (DACs) intermittently for years until the problem was isolated. The ICs failed a reference voltage test where the voltage fluctuated as a function of the power supply voltage. These components would then recover when decapsulated or x-rayed. Again, the situation occurred because of triboelectric charging.



Figs. 6-9: Current-voltage (I-V) curves (top), silicon-silicon dioxide band diagram for basic EPROM structure (bottom), and triboelectric charging potential for various materials (right).

Announcements

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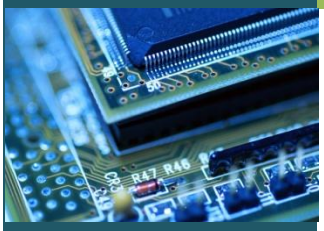

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Ask the Experts

Q: Why is Latchup testing sometimes performed at high temperatures?

Latchup depends on temperature, as shown by several studies of electrically induced latchup by Shoucair and Kolasinsky. The triggering current for electrically induced latchup decreases more than a factor of two as the temperature of latchup test structures is increased from 300 to 400 K. The main reason for this dependence is the increase in well resistance (it approximately doubles), with some additional contribution from the decreased forward voltage at high temperature.

To post, read, or answer a question, visit http://forums.semitracks.com/.
We look forward to hearing from you!

Technical Tidbit

[Measuring with the Scanning Laser Microscope or Other Optical Tools]

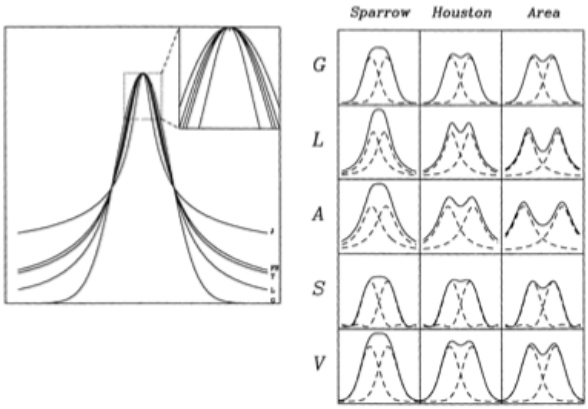
Developed by Lord Rayleigh in 1879, the Rayleigh criteria is the oldest method to resolve distances between two identical, diffraction-limited point sources with the aid of Bessel functions. The criterion is $1.22f\lambda/L$, where f is the focal ratio of the imaging system. It was intended for use on in this context, but is widely used because of its simplicity.

A second criterion is the Sparrow criterion, which depends on the property of the summed line profiles. As the lines move closer together, a minimum develops. Sparrow suggested that a natural definition of resolution is where the saddle point first develops, or when the gradient at the peak of the summed profile is zero.

The third criterion is the Houston criterion. The Houston criterion is a standard metric in Astronomy for defining spectral purity. It is defined as the Full-width-at-Half-Maximum (FWHM) of the Line Spread Function (LSF). Some groups that work in failure analysis suggest that this criterion is a good technique for optical resolution, and we agree.

A fourth criterion that has been proposed is the equivalent width criterion, or the area of the line profile divided by the peak height. While there are some compelling advantages to using the equivalent width criterion, it is not well known.

We show several of these criteria in graphic form in the figure below.



The figure shows five common functions with the same Full-width-Half-Maximum that show a transition from core power to wing power from Gaussian through Lorentzian, $x^{-1}\tanh(x)$, Fraser-Suzuki, to A.W. Jones. The table on the right shows the different possible criteria for the resolution of two identical instrumental functions: (G) Gaussian, (L) Lorentzian, (A) Airy, (S) sinc^2, and (V) Voigt. The Equivalent Width (Area) criterion is shown on the right.

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