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Basic ATPG Diagnosis

By Christopher Henderson

This section provides an introduction to ATPG Diagnosis. ATPG Diagnosis uses the ATPG circuitry, tester, and test results to help isolate the location of a failure on a complex chip. We will describe the process flow and some concerns one must take into account.

A brief comment is in order on terminology. We will want to differentiate between "ATPG" and "ATPG diagnosis." Not just because the actual pattern generation and the diagnosis of ATPG patterns may be performed with different tools/products, but because there are some subtle but important differences. For instance, during pattern generation you may only target stuck-at faults, since a pattern targeting stuck-at faults will typically detect bridge and open defects. For diagnosis however, you would typically also have models for bridges and opens, even though these models weren't needed for pattern generation.

In this Issue:

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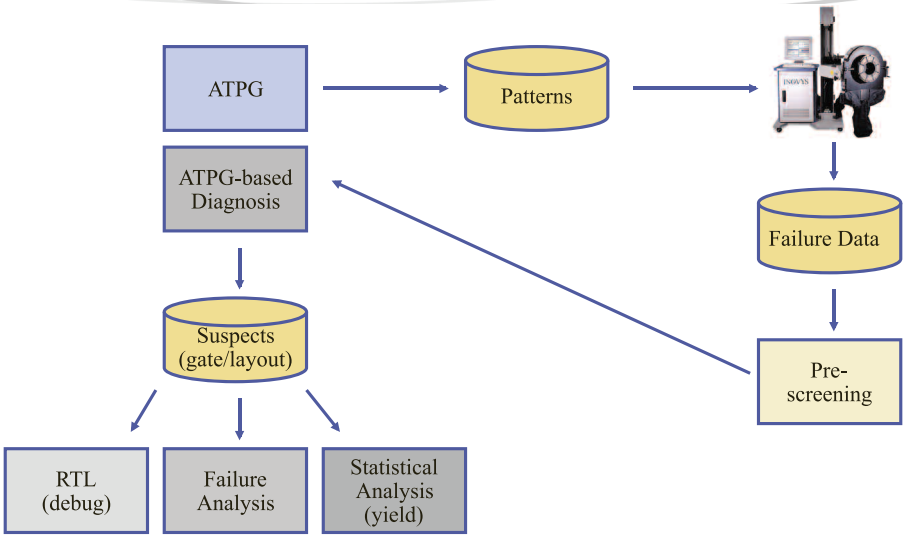


Figure 1. Scan-based diagnosis flow.

Here's how the process works (Figure 1). During the design phase, design and test engineers run automatic test pattern generation software to generate test vectors that will theoretically exercise the majority of the nodes within the circuit. These patterns can be input into a tester. The tests can be run on a part or group of parts to identify failures. These failures can then be analyzed for trends or severity. If the production contract or other issues dictate that the parts should be analyzed, they can be run through an ATPG-based diagnosis process. With models for opens and bridges, one can use ATPG-based diagnosis to identify suspect nodes based on the layout and failing vectors. One can make further use of the data for debug, failure analysis, and statistical analysis.

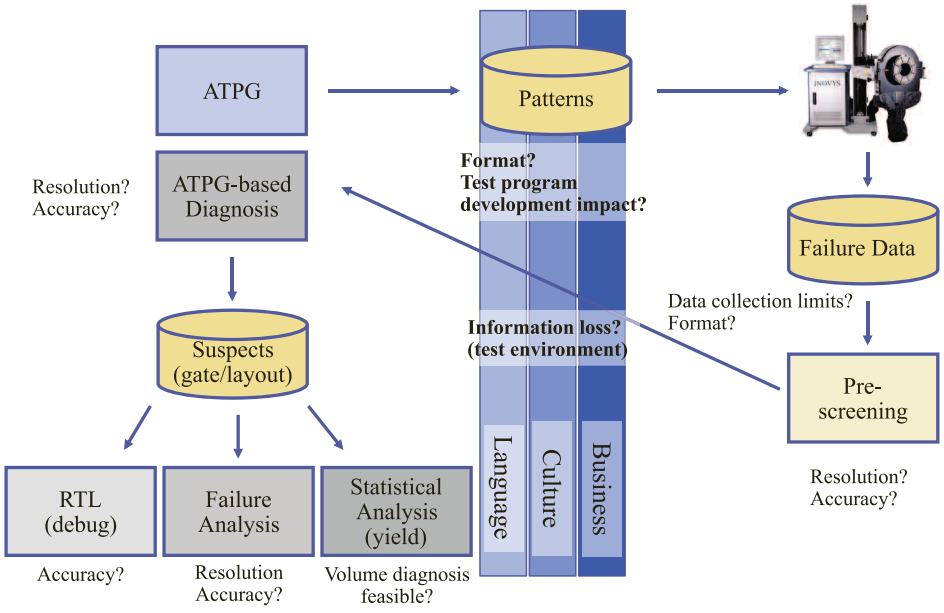


Figure 2. Scan-based diagnosis flow challenges.

There are challenges associated with this process aside from the time and effort to set it up (Figure 2). These include formats for patterns, impacts to test program developments, data collection limits, resolution, accuracy, and the feasibility of volume diagnosis. These impacts cut across business, culture, and language. Let's look into some of the challenges in more detail.

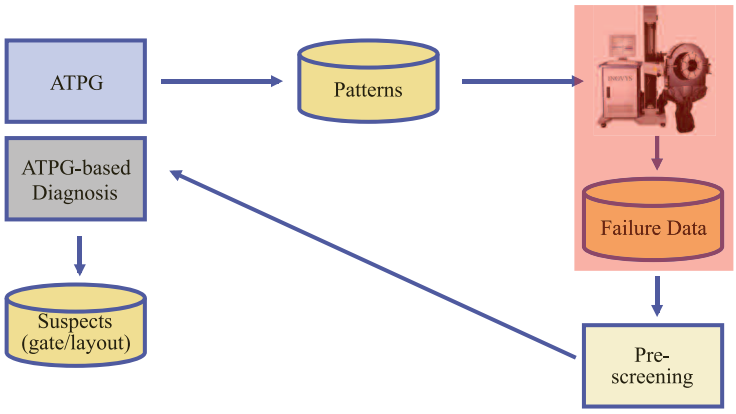


Figure 3. Scan-based diagnosis requirements (enough failure data).

The first issue is the ability to collect enough failure data (Figure 3). ATE vector sets for modern ICs are quite large. Full functional test vector sets can run into the millions of vectors. Even structural vector sets based solely on scan chain testing generate enormous amounts of data. This makes these tests impractical for in-situ debug on a production test floor. If one does use the test floor for debug, there is likely to be a test time impact for volume applications.

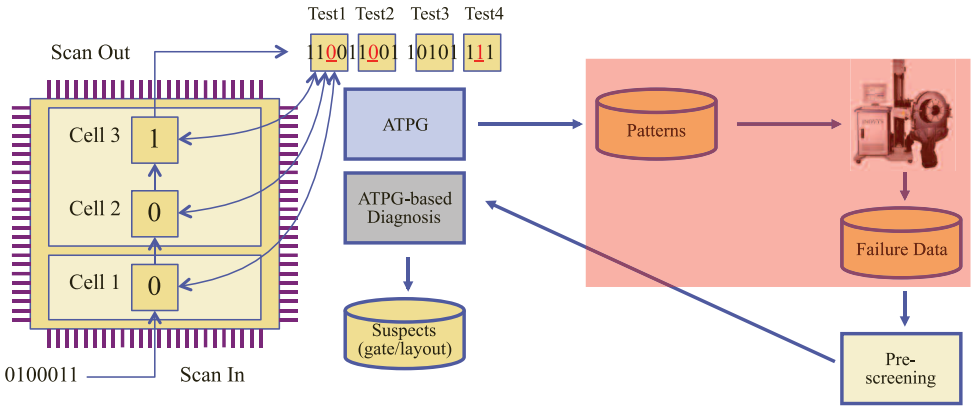


Figure 4. Scan-based diagnosis requirements (formats).

A second major problem is that of formats. The failure data needs to be in a format that the diagnosis tool can recognize. One must be able to identify each scan pattern and map the data onto the scan cells. From a practical standpoint this means working within a particular vendor's tool flow, or spending time developing routines to translate between formats.

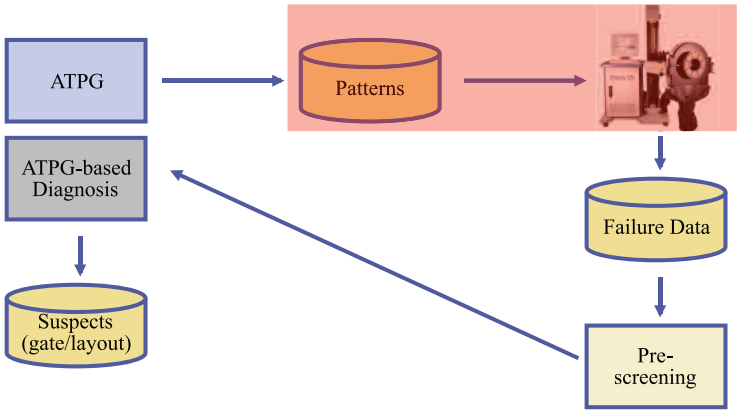


Figure 5. Scan-based diagnosis requirements (production test vs. ATPG).

Another problem is the generation of a production-ready vector set. While ATPG can generate the ones and zeroes to detect certain types of failures, further work must be done to generate a working test program. One must add initialization vectors. One must cyclize the vectors, that is, turn them into patterns with an appropriate clock cycle and the correct delays. Other factors include merging multiple patterns into a single test set, merging core or block-level patterns into top-level patterns, and running through pattern translation.

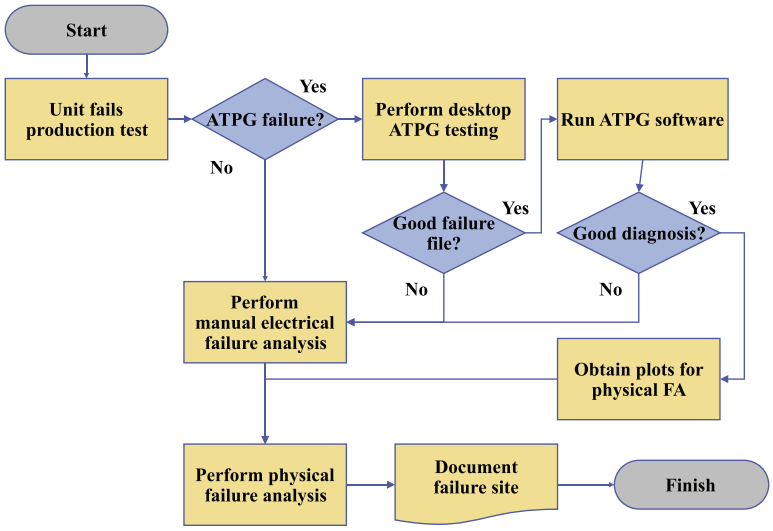


Figure 6. Flowchart for ATPG diagnosis process.

Figure 6 illustrates the basic flowchart for the Automatic Test Pattern Generation Diagnosis Process. Once the device has been verified as a failure, the scan chains must be verified. If the failure affects the scan chains, then the results of the fault simulation will be inaccurate. Normally, the software simulates selected faults to determine the set of faults whose simulated failures most closely match the actual failure. In the case of a real failure, we instead perform desktop ATPG testing using a less expensive structural or scan test system and capture a failure file. If the file contains observable failures, then the ATPG software can be run and compared against the desktop ATPG results. If the ATPG software results yield a good diagnosis, then one can bypass the time-consuming manual fault isolation activity. One can simply obtain the plots of the suspect nodes and go directly to the physical characterization step.

Technical Tidbit

Refreshing the Memory

Since DRAM memory cells are capacitors, the charge they contain can leak away over time. If the charge is lost, so is the data. To prevent this from happening, DRAMs must be refreshed—that is, the charge on the individual memory cells must be restored periodically. The frequency with which refresh must occur depends on the silicon technology used to manufacture the memory chip and the design of the memory cell itself.

Reading or writing a memory cell has the effect of refreshing the selected cell. Unfortunately, not all cells are read or written within the time limitations. Thus each cell in the array must be accessed and restored during the refresh interval. In most cases, refresh cycles involve restoring the charge along an entire row. Over the course of the entire interval, every row is accessed and restored. At the end of the interval, the process begins again.

System designers have a lot of latitude in designing and implementing memory refresh. They may choose to fit refresh cycles between normal read and write cycles, or they may decide to run refresh cycles on a fixed schedule, forcing the system to queue read and write operations when they conflict with refresh requirements.

There are several different ways to refresh a memory array. The method you use will depend on the memory product you choose and the requirements of the system you are designing. Three common refresh options are briefly described below. Another refresh option is hidden refresh, in which a read or write operation and a refresh cycle are performed during a single $\overline{CAS}$ active period.

Using $\overline{RAS}$ Only Refresh (ROR)

Normally, DRAMs are refreshed one row at a time. The refresh cycles are distributed across the entire refresh interval in such a way that all rows are refreshed within the required interval. To refresh one row of the memory array using $\overline{RAS}$ Only Refresh, the following steps must occur.

1. The row address of the row to be refreshed must be applied at the address input pins.
2. $\overline{RAS}$ must switch from high to low. $\overline{CAS}$ must remain high.
3. At the end of the required amount of time, $\overline{RAS}$ must return high.

Using $\overline{CAS}$ before $\overline{RAS}$ Refresh (CBR)

To refresh one row of the memory array using $\overline{CAS}$ before $\overline{RAS}$ Refresh, the following steps must occur.

1. $\overline{CAS}$ must switch from high to low.
2. $\overline{WE}$ must switch to a high state (Read).
3. After the prescribed delay, $\overline{RAS}$ must switch from high to low.

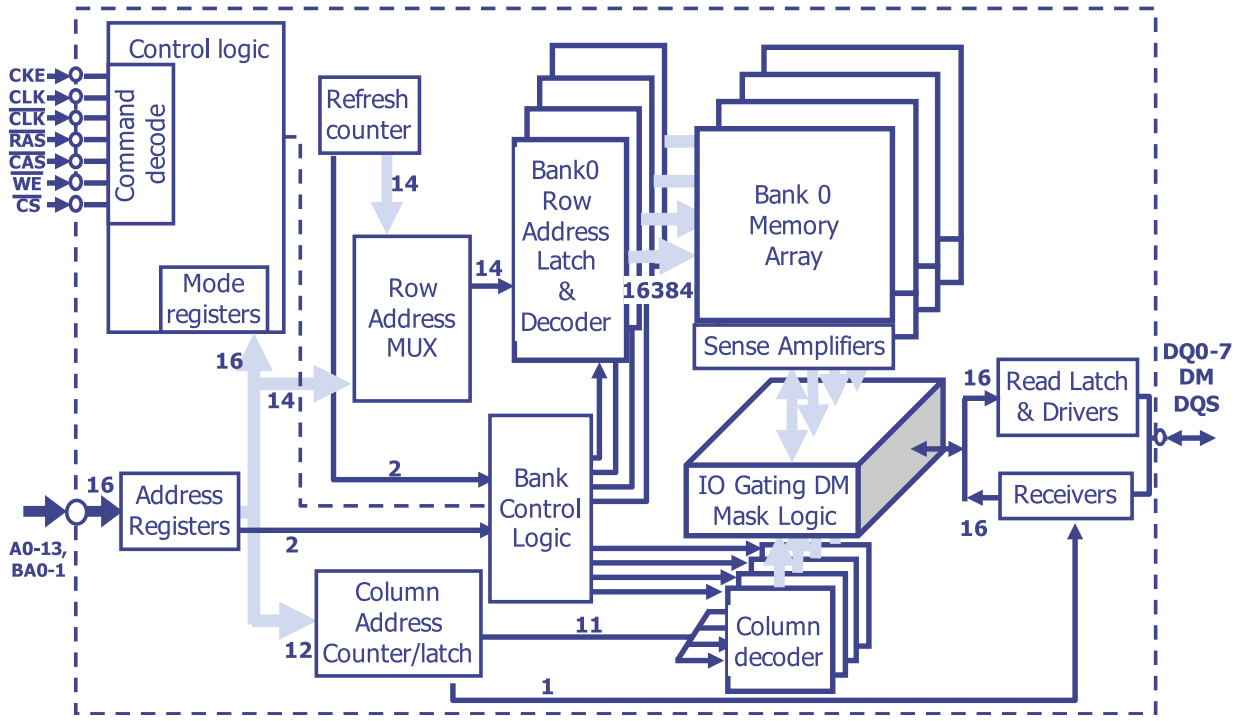
4. An internal counter determines which row is to be refreshed.
5. After the required delay, $\overline{CAS}$ returns to a high level.
6. After the required delay, $\overline{RAS}$ returns to a high level.

The main difference between ROR and CBR is the method for keeping track of the row address to be refreshed. With ROR, the system must provide the row address to be refreshed. With CBR, the chip keeps track of the addresses using an internal counter.

Self Refresh (SR)

Self Refresh, also referred to as Sleep Mode or Auto Refresh, is unique because it uses an on-chip oscillator to determine the refresh frequency and a counter to keep track of addressing. SR is most often used for battery-powered mobile applications and applications that use a battery for backup power. While in sleep mode, the device uses extremely low current.

The timing required to initiate SR is a CBR cycle with $\overline{RAS}$ active for a minimum of 100 microseconds. The length of time that a device can be left in sleep mode is limited by the power source used. To exit, $\overline{RAS}$ and $\overline{CAS}$ are brought high.



Ask the Experts

Q: We are looking to do tests in RGA system that can work in deep vacuum. Do you know of someone that can conduct such tests?

A: There are a number of labs that can do this. Here are three that can perform this type of testing.

Pernicka - www.pernicka.com
Oneida Research Services - www.orslabs.com
Riga Analytical Labs - www.rigalab.com

Again, this is not meant to be an exhaustive list; there are others as well.

Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of wafer fab processing.
5. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Module 1: Basics & Fundamentals; Semiconductor Devices and ICs
    a. Acronyms
    b. Common Terminology
    c. Brief History
    d. Semiconductor Materials
    e. Electrical Conductivity
    f. Semiconductor Devices
    g. Classification of ICs & IC Processes
    h. Integrated Circuit Types
2. Module 2: Crystallinity, Crystal Defects, Crystal Growth
    a. Crystallinity
    b. Crystal Defects
    c. Crystal Growth
    d. Controlling Crystal Defects
3. Module 3: Basic CMOS Process Flow
    a. Transistors and Isolation
    b. Contacts/Vias Formation
    c. Interconnects
    d. Parametric Testing
4. Module 4: Ion Implantation 1 (The Science)
    a. Doping Basics
    b. Ion Implantation Basics
    c. Dopant Profiles
    d. Crystal Damage & Annealing

5. Module 5: Ion Implantation 2 (Equipment, Process Issues)
    a. Equipment
    b. Process Challenges
    c. Process Monitoring & Characterization
    d. New Techniques

Day 2

6. Module 6: Thermal Processing
    a. Overview of Thermal Processing
    b. Process Applications of SiO2
    c. Thermal Oxidation
    d. Thermal Oxidation Reaction Kinetics
    e. Oxide Quality
    f. Atomistic Models of Thermal Diffusion
    g. Thermal Diffusion Kinetics
    h. Thermal Annealing
    i. Thermal Processing Hardware
    j. Process Control
7. Module 7: Contamination Monitoring and Control
    a. Contamination Forms & Effects
    b. Contamination Sources & Control
    c. Contamination Characterization & Measurement
8. Module 8: Wafer Cleaning
    a. Wafer Cleaning Strategies
    b. Chemical Cleaning
    c. Mechanical Cleaning
9. Module 9: Vacuum, Thin Film, & Plasma Basics
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics
10. Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
    a. CVD Basics
    b. LPCVD Films
    c. LPCVD Equipment
    d. Epi Basics
    e. Epi Process Applications
    f. Epi Deposition Process
    g. Epi Deposition Equipment

Day 3

11. Module 11: PVD
    a. PVD (Physical Vapor Deposition) Basics
    b. Sputter Deposition Process
    c. Sputter Deposition Equipment

d. Al-Based Films
e. Step Coverage and Contact/Via Hole Filling
f. Metal Film Evaluation

12. Module 12: Lithography 1 (Photoresist Processing)
    a. Basic Lithography Process
    b. Photoresist Materials
    c. Photoresist Process Flow
    d. Photoresist Processing Systems
13. Module 13: Lithography 2 (Image Formation)
    a. Basic Optics
    b. Imaging
    c. Equipment Overview
    d. Actinic Illumination
    e. Exposure Tools
14. Module 14: Lithgroaphy 3 (Registration, Photomasks, RETs)
    a. Registration
    b. Photomasks
    c. Resolution Enhancement Techniques
    d. The Evolution of Optical Lithography
15. Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
    a. Etch Basics
    b. Etch Terminology
    c. Wet Etch Overview
    d. Wet Etch Chemistries
    e. Types of Dry Etch Processes
    f. Physics & Chemistry of Plasma Etching

Day 4

16. Module 16: Etch 2 (Dry Etch Applications and Equipment)
    a. Dry Etch Applications
    b. SiO2
    c. Polysilicon
    d. Al & Al Alloys
    e. Photoresist Strip
    f. Silicon Nitride
    g. Dry Etch Equipment
    h. Batch Etchers
    i. Single Wafer Etchers
    j. Endpoint Detection
    k. Wafer Chucks

17. Module 17: CVD 2 (PECVD)
    a. CVD Basics
    b. PECVD Equipment
    c. CVD Films
    d. Step Coverage
18. Module 18: Chemical Mechanical Polishing
    a. Planarization Basics
    b. CMP Basics
    c. CMP Processes
    d. Process Challenges
    e. Equipment
    f. Process Control
19. Module 19: Copper Interconnect, Low-k Dielectrics
    a. Limitations of "Conventional" Interconnect
    b. Copper Interconnect
    c. Cu Electroplating
    d. Damascene Structures
    e. Low-k IMDs
    f. Cleaning Cu and low-k IMDs
20. Module 20: Leading Edge Technologies & Techniques
    a. Process Evolution
    b. Atomic Layer Deposition (ALD)
    c. High-k Gate and Capacitor Dielectrics
    d. Ni Silicide Contacts
    e. Metal Gates
    f. Silicon on Insulator (SOI) Technology
    g. Strained Silicon
    h. Hard Mask Trim Etch
    i. New Doping Techniques
    j. New Annealing Techniques
    k. Other New Techniques
    l. Summary of Industry Trends

References:

Wolf, Microchip Manufacturing,
Doering & Nishi, Semiconductor Manufacturing Technology, 2nd ed.
Wolf, Silicon Processing, Vol. 4
Wolf, Silicon Processing, Vol. 1, 2nd ed.

DESIGN AUTOMATION CONFERENCE 54

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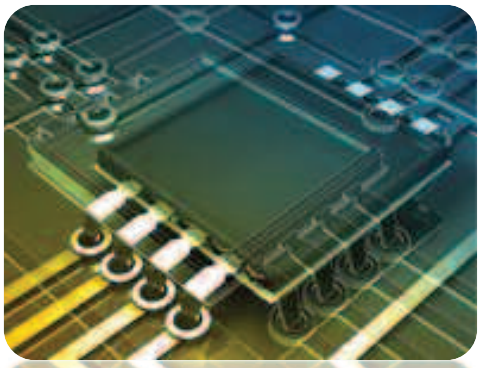
Semitracks will be at the Si2.org booth, and would be happy to discuss training needs, and creating training materials for your userbase.
Contact us at info@semitracks.com during the conference!



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We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Defect Based Testing
May 3 – 4, 2017 (Wed – Thur)
Munich, Germany

Failure and Yield Analysis
May 8 – 11, 2017 (Mon – Thur)
Munich, Germany

Semiconductor Reliability and Qualification
May 15 – 18, 2017 (Mon – Thur)
Munich, Germany

Semiconductor Statistics
May 22 – 23, 2017 (Mon – Tue)
Munich, Germany

Wafer Fab Processing
June 5 – 8, 2017 (Mon – Thur)
Portland, Oregon, USA