Issue 138 December 2020

InfoTracks

Semitracks Monthly Newsletter

Resistors

By Christopher Henderson

This month, we will begin a new series of Feature Articles that will cover resistors. Resistors are ubiquitous, even in today's advanced electronics. They play an integral role in signal integrity, protection, and signal formation. This is the first of five articles and will cover the taxonomy and types of resistors.

Component suppliers manufacture resistors in several different formats. They include composition, metal or carbon film, thin film, thick film, and wire-wound. There are various physical implementations of these components. At higher frequencies, resistors are used with high frequency connectors to form attenuators. We should also note that thermistors are resistors having a known, calibrated response to changes in temperature since temperature can be monitored by measuring resistance.

In Figure 1, we show resistors by their taxonomy. Resistors can be divided into two major groupings: linear and non-linear. The non-linear group contains devices such as thermistors, photo-resistors, varistors, and surface mount devices. Linear resistors can be further divided into fixed and variable groupings. Variable resistors include potentiometers, rheostats, and trimmers. The fixed resistor category is the biggest, and includes carbon composition resistors, wire-wound resistors, thick film and thin film resistors. There are other sub-groups beyond what we will discuss in this and future articles, but these are the major ones.

In this Issue:

Page 1	Resistors
Page 4	Technical Tidbit
Page 5	Ask the Experts
Page 6	Spotlight
Page 9	Upcoming Courses

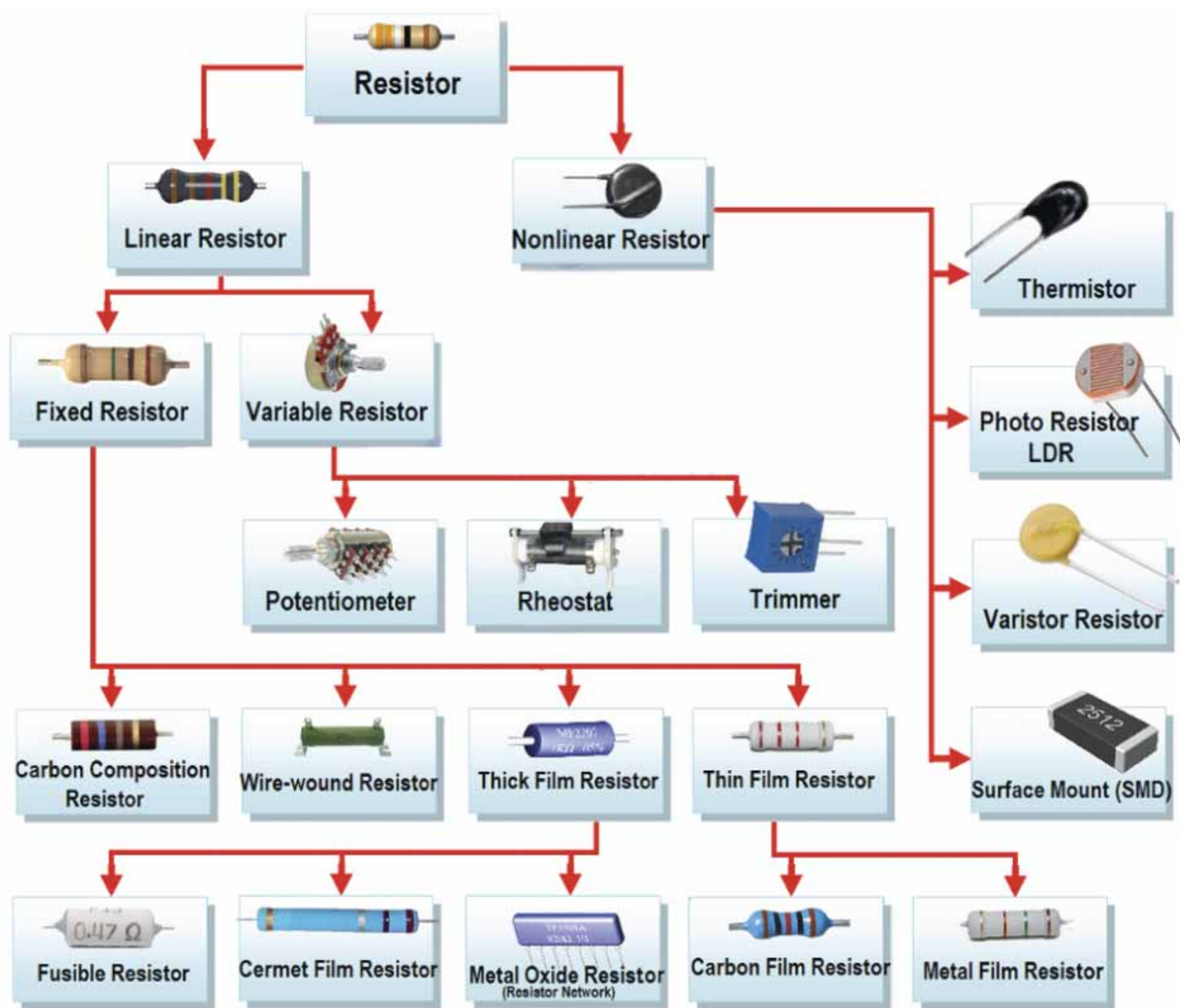


Figure 1. Taxonomy of resistors (Courtesy of www.electricaltechnology.org).

We can also divide resistors by application type. As shown in Figure 2, some major groupings would include surface mount resistors, leaded resistors, high power resistors, high voltage resistors, current sense and shunt resistors, precision resistors, custom resistors, wire-wound resistors, and pulse protection resistors.

Figure 2. Types of resistors.

In next month's Feature Article, we will go into more detail on the Composition Resistor which is part of the Fixed Resistor category.

Technical Tidbit

Tunneling Through Thin Dielectrics

As the channel length is reduced, the oxide thickness must also be reduced to maintain a steady increase in performance and circuit density, while suppressing short-channel effects. The ratio of channel length to gate oxide thickness must remain above approximately 45 to 1. An oxide film thinner than about 4 nm is referred to as an ultra-thin oxide. Assuming a maximum allowable field for this thickness of 6×10^6 V/cm, the maximum voltage that can be applied across a 4-nm oxide is 2.4V. As the oxide thickness is reduced below 4 nm, the probability for direct tunneling through the oxide increases rapidly. For example, for an effective channel length of 70 nm, the oxide thickness must drop to about 1.5 nm. For such a thickness, the gate tunneling current can increase to above 10 A/cm^2, where the generated power becomes prohibitive. Another disadvantage of using ultra-thin oxide as a gate dielectric in PMOS is that it allows the penetration of boron from the P^+-gate into silicon. The primary motivation for the development of high-dielectric constant (high-**κ**) gate insulators is to increase the physical dielectric thickness, reducing tunneling, while maintaining an ultra-thin equivalent oxide thickness. An insulator of dielectric constant 20 and of thickness 7.7 nm has an equivalent oxide thickness 7.7 times the ratio of dielectric constants (3.9 divided by 20), which is equal to 1.5 nm, as shown by the equation in Figure 1.

$$t_{eq} = \frac{\varepsilon_{ox}}{\varepsilon_{high-\kappa}} t_{high-\kappa} = \frac{3.9}{20} \times 7.7 \cong 1.5 \quad \text{nm}$$

Figure 1. Equivalent oxide thickness.

The thickness of silicon dioxide as a gate dielectric cannot be scaled below approximately 1.5 nm because of the very high tunneling gate current. For the same equivalent oxide thickness, the physical dielectric thickness can be increased, and the tunneling probability reduced by increasing the dielectric constant. Referring to Figure 2, for an equivalent oxide thickness of 1.5 nm, the tunneling gate current through a gate dielectric of dielectric constant 18 is about 250 times smaller than the gate current through silicon dioxide.

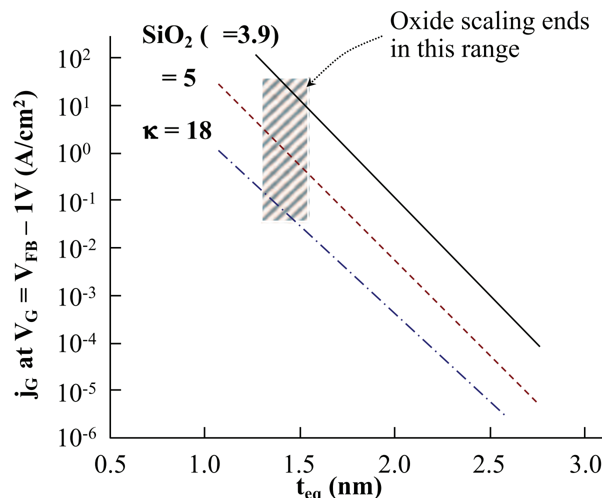


Figure 2. Comparison of tunneling current density for three gate dielectrics of different dielectric constants and same equivalent oxide thickness.

To learn more about this topic, you can register for our Advanced Device Physics Course online at: https://www.semitracks.com/online-training/premium-courses/advanced-device-physics

Ask the Experts

Q: Why is Laser Dicing becoming popular?

A: There are several reasons: one, laser dicing is less likely to cause thin-film damage on the wafer; two, laser dicing does not use a significant amount of consumable items like deionized water and saw blades; and three, laser dicing does not require a wide kerf, so more circuits can be manufactured on a wafer.

Learn from the Experts...
...wherever you are.

-Learn at your own pace.
-Eliminate travel expenses.
-Personalize your experience.
-Search a wealth of information.
Visit us at www.semitracks.com for more information.

SEMITRACKS, INC.
Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

Spotlight: Advanced CMOS/FinFET Fabrication

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" Advanced CMOS/ FinFET Fabrication is a 1-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

WHAT WILL I LEARN BY TAKING THIS CLASS

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs and FD-SOI are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including ion implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.
2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.
3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.
4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of SOI technology and the technical issues.
2. Participants will understand how Hi-K/Metal Gate devices are manufactured.
3. Participants will also understand how FinFET devices are manufactured.
4. The seminar provides a look into the latest challenges with copper metallization and Low-k dielectrics.
5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.
6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.
7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.
8. Finally, the participants see a comparison between FD-SOI (the leading alternative) and FinFETs.

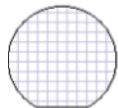
COURSE OUTLINE

1. Advanced CMOS Fabrication – Introduction
2. Front End Of Line (FEOL) Processing
    a. SOI and FD-SOI
    b. Ion Implantation and Rapid Thermal Annealing
    c. Pulsed Plasma Doping
    d. Hi-K/Metal Gates
    e. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
3. Back End Of Line (BEOL) Processing
    a. Introduction and Performance Issues
    b. Copper
        i. Deposition Methods
        ii. Liners
        iii. Capping Materials
        iv. Damascene Processing Steps
    c. Lo-k Dielectrics
        i. Materials
        ii. Processing Methods
    d. Reliability Issues

4. FinFET Manufacturing Overview
    a. Substrates
        i. Bulk
        ii. SOI
    b. FinFET Types
    c. Process Sequence
    d. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
5. FinFET Reliability
    a. Defect density issues
    b. Gate Stack
    c. Transistor Reliability (BTI and Hot Carriers)
    d. Heat dissipation issues
    e. Failure analysis challenges
6. Future Directions for FinFETs
    a. Comparison of FD-SOI and FinFETs – Are FinFETs a better choice?
    b. Scaling

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

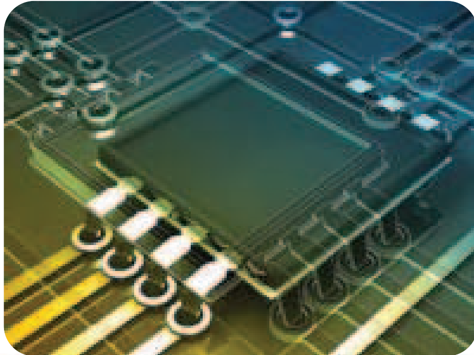
Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



SEMITRACKS INC.

Semiconductor, Microelectronics, Microsystems and Nanotechnology Training

6501 Wyoming NE, Suite C215
Albuquerque, NM 87109-3971
Tel. (505) 858-0454
Fax (866) 205-0713
e-mail: info@semitracks.com



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

~

For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Webinars

(Click on each item for details)

Failure and Yield Analysis

WEBINAR—4 sessions of 4 hours each
Europe: February 1 – 4, 2021 (Mon – Thur),
1:00 P.M. – 5:00 P.M. CET
US: February 1 – 4, 2021 (Mon – Thur),
9:00 A.M. – 1:00 P.M. PST

Semiconductor Reliability / Product Qualification

WEBINAR—4 sessions of 4 hours each
Europe: February 8 – 11, 2021 (Mon – Thur),
1:00 P.M. – 5:00 P.M. CET
US: February 8 – 11, 2021 (Mon – Thur),
9:00 A.M. – 1:00 P.M. PST

Wafer Fab Processing

WEBINAR—4 sessions of 4 hours each
Europe: April 6 – 9, 2021 (Tue – Fri),
1:00 P.M. – 5:00 P.M. CET
US: April 19 – 22 (Mon – Thur),
9:00 A.M. – 1:00 P.M. PST

IC Packaging Technology

WEBINAR—4 sessions of 4 hours each
Europe: April 19 – 22, 2021 (Mon – Thur),
1:00 P.M. – 5:00 P.M. CET
US: April 12 – 15, 2021 (Mon – Thur),
9:00 A.M. – 1:00 P.M. PST

Advanced CMOS/FinFET Fabrication

WEBINAR—4 sessions of 2 hours each
Europe: April 26 – 29, 2021 (Mon – Thur),
3:00 P.M. – 5:00 P.M. CET
US: April 5 – 8, 2021 (Mon – Thur),
9:00 A.M. – 11:00 A.M. PST