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YOUR QUARTERLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Transfer Molding

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In this quarter's Feature Article, we continue our series on Transfer Molding. Transfer Molding is one of the more common steps in semiconductor packaging, and provides protection for the sensitive semiconductor components and packaging interconnect. We will continue our discussion of transfer molding by focusing on the mold compound manufacturing process, some issues with mold compound materials, and molding advanced packages.

Let's briefly discuss the epoxy resin mold compound manufacturing process. We show this process graphically in Figure 1. The resin, hardener, filler material, and additives are first run through a mixing process, and then through a heating and kneading process to create a more uniform mixture. After this step, the epoxy resin mold compound material is cooled, and then pulverized into a powder. There is then a post-mixing step, followed by a step to turn the powder into a pellet or tablet, which is the common delivery form for the transfer molding process.

WHAT'S INSIDE?

Want to take control of your learning? See page 8

Upcoming Courses:

- Defect Based Testing
- Wafer Fab Processing
- Failure and Yield Analysis
- Reliability and Product Qualification
- EOS, ESD and How to Differentiate

See page 12 for more details

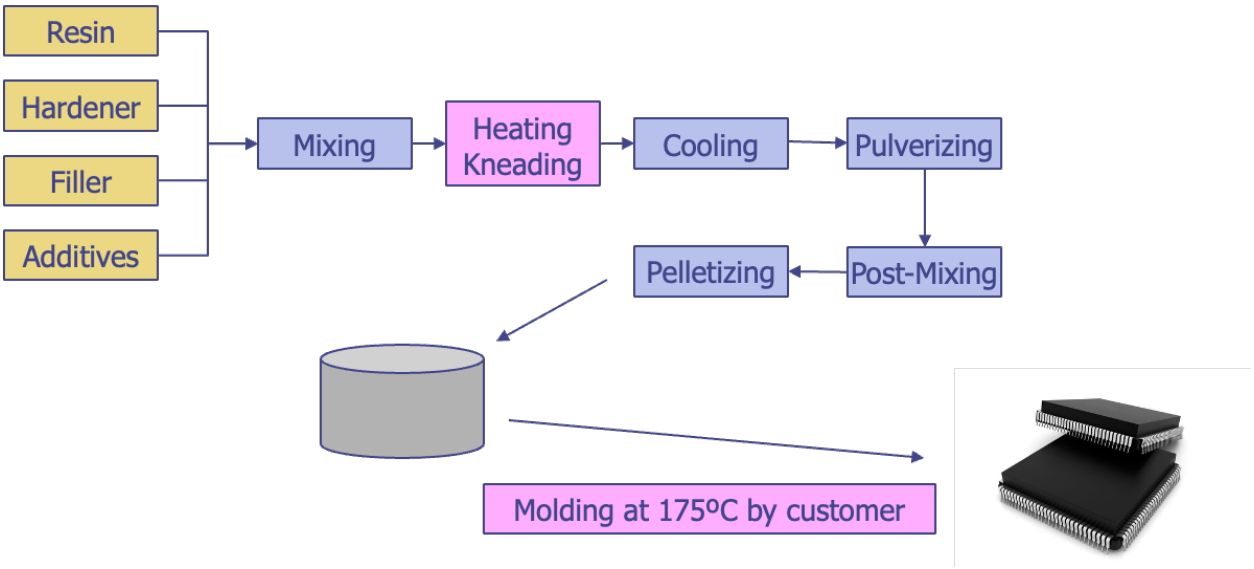

Figure 1- Depiction of the mold compound manufacturing process.

The particulate matter in mold compound typically comes in two forms: flake and spherical. In Figure 2, we show an image of flake silica on the left, and spherical, or colloidal, silica on the right. Flake silica is used in low-cost epoxy resin mold compounds, but it creates pin point stresses that induce passivation overcoat cracks on the die surface. Furthermore, flake silica can create issues during the injection process, such as increased viscosity, non-uniform flow, and wire sweep issues. Spherical silica tends to cause fewer problems, but is more expensive to include as a filler material in epoxy resin mold compounds.

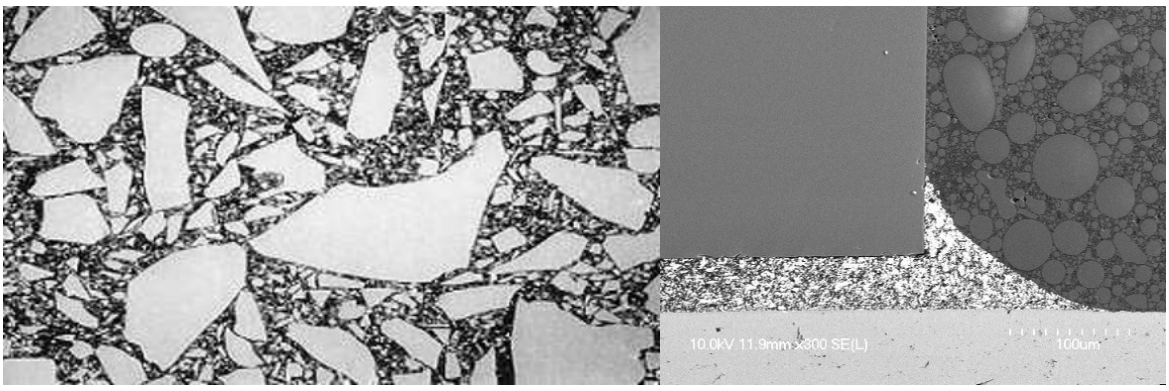

Figure 2- Flake silica – used in low-cost mold compounds (left), and spherical (or colloidal silica) – used for improved reliability (right).

Increased wire density and wire length in stack die packages make molding stack packages more difficult than conventional single-die packages. For example, different layers of wire bond loops, subjected to varying amounts of drag force, can result in differences in wire sweep. This increases the possibility of wire shorts. Furthermore, the various gaps between the components make it more difficult to remove all of the voids and achieve a balanced flow with the mold fluid.

When dealing with stacked die packages, engineers require additional epoxy resin mold compound material development, runner gate design, and wire layout optimization to achieve better yield in molding. For example, low-viscosity compounds, smaller filler size compounds, and slower transfer speeds reduce problems with wire sweep. A top runner gate design is more desirable than a corner gate in reducing wire sweep, especially for long wire applications. Figure 3 shows the placement of the corner gate, and the placement of the top gate.

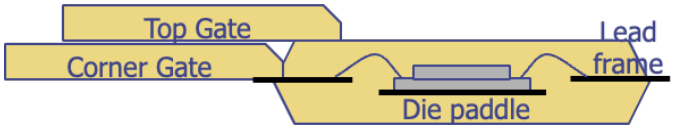

Figure 3- Graphic showing the placement of a Top Gate and a Corner Gate, with respect to the mold cavity for the package.

One method for handling some of these issues is through wire loop construction and placement. A lateral worked loop trajectory also reduces mold sweep by pre-deforming the wire in anticipation of the sweep direction. Molding experiments showed decreased wire sweep with this loop trajectory. On average, the molding sweep was reduced by nearly 50%. Folded forward looping can also reduce molding sweep by reducing excess wire in the loop, and by eliminating the heat-affected zone by folding the heat-affected region. The heat-affected zone is the weakest region along wire that is subject to epoxy resin mold compound sweep.

After the molding process in the molding system, the packages undergo a post mold cure. This is performed after de-gating and culling to ensure the epoxy resin mold compound is fully cured. The post mold cure condition is typically around 175ºC for 4 to 6 hours, excluding the ramp up and ramp down time for the oven. In Figure 4, we show an example of a package where lateral worked loop trajectory is employed, and images of the Heat Affect Zones for two gold wire samples.

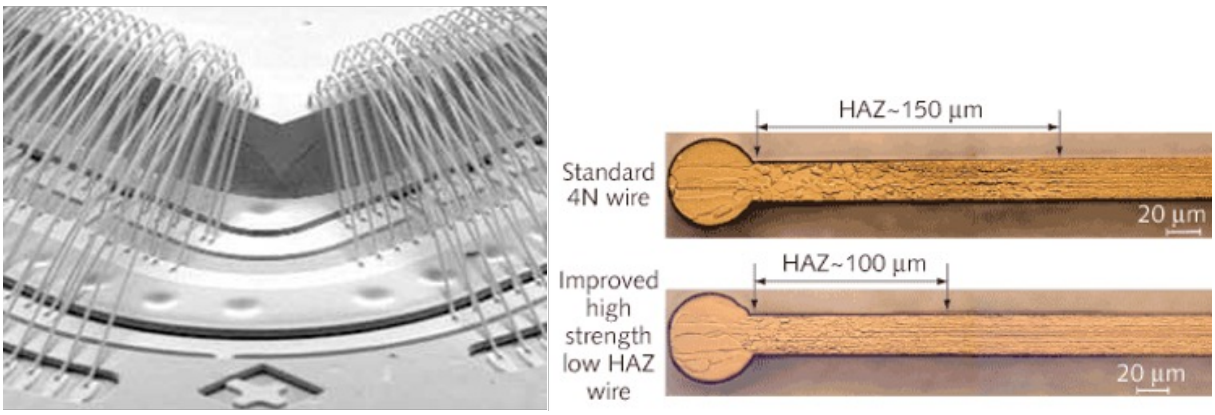

Figure 4- Package with lateral loop trajectory bonding (left), and Heat Affected Zones in gold wire (right).

Selecting the package materials, and in particular, the epoxy resin mold compound, is an important piece of the package design and engineering process. We know that the package will possibly contain a lead frame, and or wires, solder bumps or pillars. We know that the package contains a polymer substrate. There will of course be one or more semiconductor chips, and in some instances, there may be ceramic materials. Therefore, the choice of epoxy resin mold compound that can best hold these materials together is a critical task. One major factor is stress. We will discuss the effect of stress in more detail in a future Feature Article.

New materials and materials-processing technologies will be needed to meet the technology requirements for the packaging and assembly of next-generation devices. With the mechanically weaker Ultra Low-κ dielectrics in the device, compatible underfill materials in the flip chip package will lessen the risk for interface stress damage to the dielectric layer. The developments of potential solutions, such as wafer level packaging and interconnect; and system in package technologies, will require materials and materials-processing innovations beyond what is available today. Figure 5 shows a table with package structural elements and potential options for these elements.

Package Structural Element	**Selected Options**		
Leadframe packages			
Leadframe metal	Alloy 42	Kovar	Copper
Wire	Gold	Aluminum	Copper
Encapsulant	Epoxy	Silicone	Polyimide
Laminate packages			
Laminate type	BT	Polyimide	High-temp FR4
Redistribution metal	Copper	Gold	Nickel
Wire	Gold	Aluminum	Copper
Encapsulant	Epoxy-molded	Epoxy-glob top	Epoxy-underfill
Wafer-level packages			
Build-up polymer	BCB	Polyimide	Epoxy
Redistribution metal	Copper	Aluminum	Gold
Encapsulant	Epoxy	Silicone	BCB
Bump contacts	Solder	Copper	Nickel gold

Figure 5- Table showing package structure elements and potential material options for those elements.

Researchers are busy developing new infrastructure for packaging materials. This corresponds to requirements coming from environmental issues such as Lead-free and Halogen-free government directives, and requirements on next-generation devices utilizing Low-κ or Ultra Low-κ. For packages utilizing Lead-free materials and Low-κ/Ultra Low-κ dielectrics, the epoxy resin mold compound and package substrate, which are the principal materials to determine package reliability level, have to be modified considering the thermomechanical stress management to adapt to Lead-free, Halogen-free, and Low-κ/Ultra Low-κ packaging. The essential property for epoxy resin mold compound and package substrates for Lead-free applications would be how they maintain sufficient heat resistance during solder reflow. Figure 6 shows a table with a partial list of banned substances for semiconductor packaging.

Lead:	Mercury:	Cadmium:	Hexavalent Chromium:	Poly Brominated Biphenyls:	Poly Brominated Diphenyl Ethers:
PB	Hg	Cd	Cr+6	PBB	PBDE

Figure 6- Table showing a partial list of banned substances for semiconductor packaging.

This leads to a dilemma with regards to epoxy resin mold compound materials. If we increase the filler content, we decrease the Coefficient of Thermal Expansion and moisture absorption. This leads to better preconditioning performance and lower package bow and warpage. However, if we increase the filler content, we increase the modulus and decrease the strength of the material. This leads to poorer moldability, and lower thermal cycling and thermal shock performance. Therefore, engineers need to pay close attention to materials and the resulting consequences of the choices they make.

In next month's Feature Article, we will continue our discussion of transfer molding by focusing on the characterization tests used to assess mold compounds.

Technical Tidbit – Ellipsometry

In this month's Technical Tidbit, we will discuss ellipsometry. Ellipsometry is a common non-destructive metrology technique used during the wafer fabrication process.

Ellipsometry is known as a specular optical technique, in other words, the angle of incidence equals the angle of reflection. The incident and the reflected beam span the plane of incidence. Light which is polarized parallel to this plane is named p-polarized. A polarization direction perpendicular is called s-polarized, accordingly. The "s" is contributed from the German "senkrecht", or perpendicular. Ellipsometry works by measuring the change in polarization state (becoming elliptical) of polarized light after it reflects off a sample, typically a thin film on a substrate. It analyzes the difference in reflection for p-polarized (parallel to the plane of incidence) and s-polarized (perpendicular) light, quantifying this change using two parameters, Psi (Ψ) and Delta (Δ). These values reveal the film's thickness, optical constants (refractive index), and surface roughness, making it a powerful, non-destructive characterization technique. The core principle is to defect a polarization change. Figure 1 helps to describe the principle of operation. An ellipsometer generates linearly polarized incident light, or basically an electric field oscillating in one plane, using a source and polarizer. This polarized light hits the sample at an oblique angle Phi (Φ), rather than vertical to the surface of the sample. The light reflects, but the p-polarized and s-polarized components reflect with different amplitudes and exhibit a phase shift. The combination of these altered components results in the reflected light having an elliptical polarization state. Next is the measurement and analysis of the refracted light. Psi (Ψ) represents the change in the amplitude ratio of the p- and s-polarized light, while Delta (Δ) represents the phase difference between the reflected p- and s-polarized light. To measure this phenomenon, an analyzer, which is basically another polarizer, and detector measure Ψ and Δ. These measured values are then compared to theoretical models (using Fresnel equations) to determine material properties like film thickness, refractive index, and density. By tracking these precise changes in polarization, ellipsometry can measure nanometer-scale features and properties, even for very thin or transparent materials, offering information beyond simple intensity measurements.

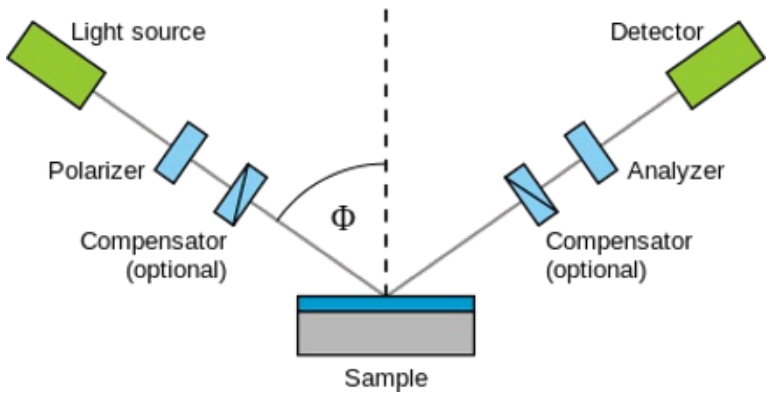

Figure 1- Principle of operation for ellipsometry.

Figure 2 shows an example of a spectroscopic ellipsometer. Electromagnetic radiation is emitted by a light source and linearly polarized by a polarizer. It can pass through an optional compensator (retarder, quarter wave plate) and falls onto the sample. After reflection, the radiation passes a compensator (optional) and a second polarizer, which is called an analyzer, and falls into the detector. Instead of the compensators, some ellipsometers use a phase-modulator in the path of the incident light beam.

Figure 2- An example of a spectroscopic ellipsometer (courtesy J.A. Woollam Co., Inc.)

Let's discuss an application. For example, on a Silicon On Insulator (SOI) wafer, the silicon and Buried Oxide (BOX) thickness can be measured by spectroscopic ellipsometry. There are two approaches to measuring the layer thickness, measuring discrete points and high-speed wafer mapping capturing a large number of points (several thousand) in one measurement pass. Mean, minimum, maximum thickness, standard deviation of silicon and BOX thickness are collected for quality monitoring. Figure 3 shows a wafer thickness map, illustrating thickness variations on a 300mm SOI wafer.

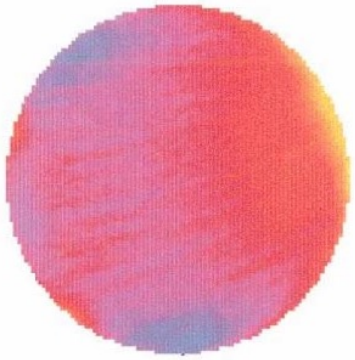

Figure 3- Wafer map of silicon layer thickness on a 300mm Silicon on Insulator (SOI) wafer.

In conclusion, ellipsometry is a fast and non-destructive method for assessing wafer fabrication processes such as thin film depositions. While the technique is not as useful on wafers that already contain complex patterns, it does work extremely well on single step process monitors.

Ask The Experts

Q: How is the etching depth controlled? Using visual inspection metrology or other techniques?

A: The etching depth is controlled mainly through understanding the etch rate. The etch rate can be experimentally determined using a Design of Experiments (DOE) approach, or through modeling and simulation. Another important technique to control the etching depth is to use an etch stop layer. The etch will proceed quickly through the material of interest but very slowly through the etch stop layer, allowing the process engineer to remove the layer of interest without removing the layers beneath it. One can use visual inspection or metrology after the etch process, but this step is mainly for the purpose of feedback to the process engineers, rather than real-time feedback.

Course Spotlight: SEMICONDUCTOR RELIABILITY AND PRODUCT QUALIFICATION

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms, and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability; assessing the impact of new materials; dealing with limited margins, and other factors. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. ***Semiconductor Reliability and Product Qualification*** is a 4-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants will learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product. This skill building series is divided into four segments:

1. **Overview of Reliability and Statistics.** Participants will learn the fundamentals of statistics, sample sizes, distributions and their parameters.

2. **Failure Mechanisms.** Participants will learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, and others.

3. **Qualification Principles.** Participants will learn how test structures can be designed to help test for a particular failure mechanism.

4. **Test Strategies.** Participants will learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The course will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.

2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.

3. The course will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.

4. The course will offer a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.

7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

DAY 1

1. Introduction to Reliability
   a. Basic Concepts
   b. Definitions
   c. Historical Information

2. Statistics and Distributions
   a. Basic Statistics
   b. Distributions (Normal, Lognormal, Exponent, Weibull)
   c. Which Distribution Should I Use?
   d. Acceleration
   e. Number of Failures

DAY 2

3. Overview of Die-Level Failure Mechanisms
   a. Time Dependent Dielectric Breakdown
   b. Hot Carrier Damage
   c. Bias Temperature Instability
   d. Electromigration
   e. Stress Induced Voiding
   f. BEOL Dielectric Reliability

4. Package Level Mechanisms
   a. Moisture/Corrosion
      i. Failure Mechanisms
      ii. Models for Humidity
      iii. Tja Considerations
      iv. Static and Periodic stresses
      v. Exercises
   b. Thermo-Mechanical Stress
      i. Models
      ii. Failure Mechanisms
   c. Chip-Package Interactions
      i. Low-k fracture
   d. Through Silicon Via Reliability
   e. Thermal Degradation/Oxidation

DAY 3

5. Board Level
   a. Package Attach (Solder) Reliability
      i. Creep/Sheer/Strain
      ii. Lead-Free Issues
      iii. Electromigration/Thermomigration
      iv. MSL Testing
   b. Board Level Reliability Mechanisms
      i. Interposer
      ii. Substrate

6. Use Condition Failure Mechanisms
   a. Electrical Overstress/ESD
   b. Radiation Effects

7. Test Structures and Test Equipment

8. Developing Screens, Stress Tests, and Life Tests
   a. Burn-In
   b. Life Testing
   c. HAST
   d. JEDEC-based Tests

DAY 4

9. Calculating Chip and System Level Reliability

10. Developing a Qualification Program
    a. Process
    b. Standards-Based Qualification
    c. Knowledge-Based Qualification
    d. MIL-STD Qualification
    e. JEDEC Documents (JESD47H, JESD94, JEP148)
    f. AEC-Q100 Qualification

11. JEDEC Tests

12. Exercises and Discussion

Upcoming Courses:

Defect-Based Testing - February 19-20, 2026 (Thurs.-Fri.) | Munich, Germany - $1,195 until Thurs. Jan. 29

Wafer Fab Processing - February 23-26, 2026 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Feb. 2

Failure and Yield Analysis - March 2-5, 2026 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Feb. 9

Semiconductor Reliability and Product Qualification - March 9-12, 2026 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Feb. 16

EOS, ESD and How to Differentiate - March 16-17, 2026 (Mon.-Tues.) | Munich, Germany - $1,195 until Mon. Feb. 23

Failure and Yield Analysis - April 13-16, 2026 (Mon.-Thurs.) | San Jose, CA - $2,095 until Mon. Mar. 23

Semiconductor Reliability and Product Qualification - April 20-23, 2026 (Mon.-Thurs.) | San Jose, CA - $2,095 until Mon. Mar. 30

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!