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InfoTracks

Semitracks Monthly Newsletter

Failure Analysis Procedures – Part III

By Christopher Henderson

This article is a continuation of last month's article. As we discussed last month, sometimes failure analyst's can best understand the FA procedure for a component by thinking about the process in terms of the type of failure. This is a flowchart that describes how to analyze an open circuit failure at either the wafer or package level.

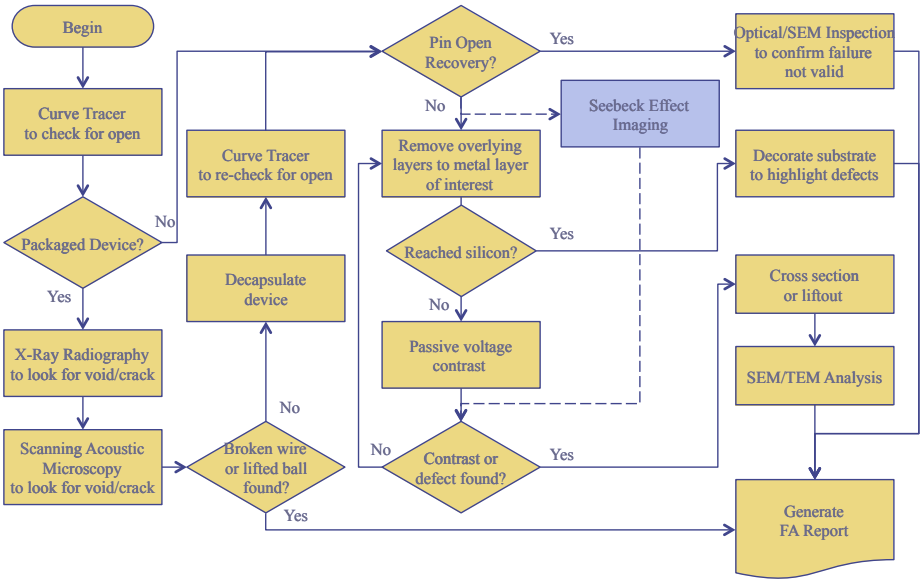

Figure 1. Flowchart for an open circuit failure.

Figure 1 shows a flowchart that describes how to analyze an open circuit. We begin by examining the device with a curve tracer

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to check for the open. The pin or bump exhibiting the open should be identifiable from the automatic test equipment (ATE) datalog for the device. If the device has not been tested it should be tested using ATE to confirm the failure. We can also do this directly with the curve tracer, but it can be very time-consuming for a device with many pins, bumps, or bond pads if we're doing this at the wafer level. The flow now branches if we have a packaged device. If we have a packaged device, we can perform x-ray radiography and scanning acoustic microscopy to look for a void or crack. There are other advanced techniques one can try like time domain reflectometry or Superconducting Quantum Interference Device (SQUID) microscopy as well to help localize this type of problem. If we are able to locate a broken wire, lifted ball, or other obvious anomaly, we can document it and proceed to the report generation. If there is no obvious defect or problem, then the problem most likely lies on the die itself. It makes sense to decapsulate the device to expose the die surface. After decapsulation, one should re-check the pin in question to make sure the open is still present. If the failure is no longer present, then an optical or SEM inspection might be in order at this point to look for anything that might have been missed. If the failure is still present, then we can begin to isolate it on the die. If the package structure is still present, we could use a laser-based technique like Seebeck Effect Imaging to localize the open. However, if the package structure is no longer present, then we will need to use a more traditional technique like passive voltage contrast. We then enter a loop where we remove overlying layers to expose the layer of interest, and perform voltage contrast. We can continue in the loop until we identify the failure site or reach the silicon substrate. Analysts use passive voltage contrast to identify opens and shorts. If we don't see incorrect contrast, then we can remove the chip layers down to the next metal layer in the node, or down to the upper-most metal layer in the next candidate. We would continue this process down through the backend of the process, or through the interconnect and dielectric layers. Once we see incorrect contrast or the defect itself, we can determine if we need further analysis. This might involve a cross-section or liftout of material. We can then examine the defect with the SEM or TEM as appropriate. If we do not see the defect after removing all of the interconnect and dielectric layers, we can decorate the substrate to highlight potential defects in the silicon. At this point, we can write up our findings in a failure analysis report.

Technical Tidbit

Rapid Thermal Processing Hardware

In this technical tidbit, we will discuss rapid thermal processing hardware. Engineers normally perform rapid thermal processing (RTP) one wafer at a time, so RTP hardware is designed to process one wafer at a time. The system rotates the wafer while in the system to minimize the effects of heating non-uniformities and gas flow non-uniformities. RTP hardware operates either at atmospheric pressure or reduced pressure, and is compatible with both dry and chlorine oxidations. Wet oxidations can be performed using in situ steam generation, where one introduces hydrogen and oxygen gas onto a hot wafer surface where they react and form steam. Obviously, the introduction of hydrogen gas in the presence of oxygen is a safety issue, and must be performed carefully with the appropriate mitigation protocols.

The manufacturers of rapid thermal processing equipment have created various designs and configurations for use in the semiconductor industry. The drawings in Figure 1 show the more common configurations. They range from quartz tube and lamps, like we show in figures A and B, to chambers with IR bulbs, rods, and hot plates, like we show in figures C, D, and E respectively. Rapid thermal annealing is fast becoming the first choice for thermal processing steps. Engineers use rapid thermal annealing for post-implant damage annealing and dopant activation, where the heat drives the dopant atoms to the lattice sites to become electrically active. They form metal silicides for contacts with the technique. Materials like titanium, cobalt, and nickel silicide lend themselves well to rapid thermal processing. Process engineers also perform rapid thermal oxidation to create thin oxide and oxynitride layers for transistor gates, capacitors, pad oxides, side wall spacers, and shallow trench isolation liners.

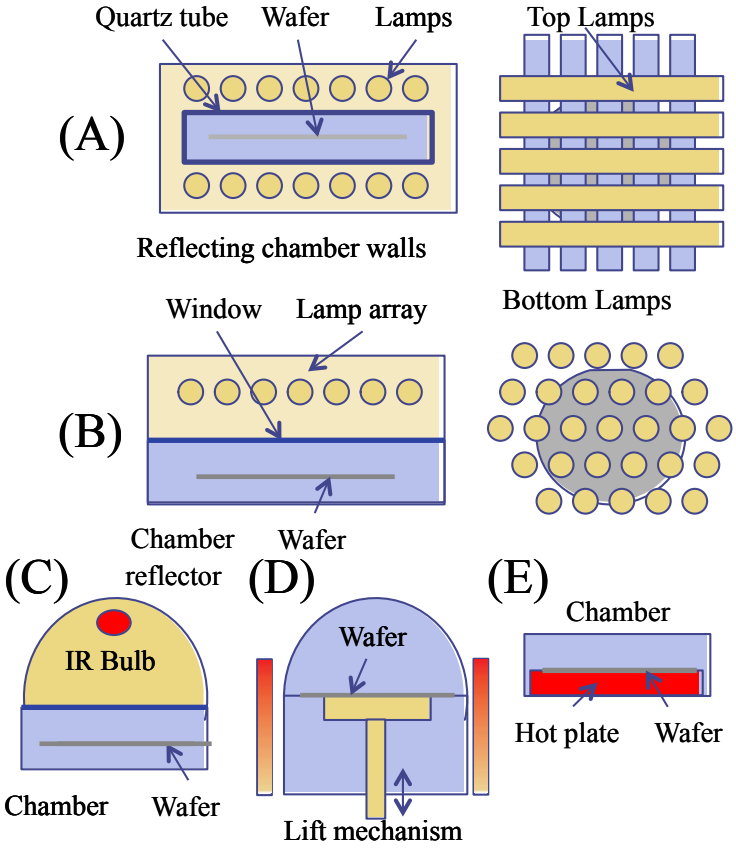

Figure 1. Common configurations for RTP hardware

Rapid Thermal Processing employs either cold wall or hall wall technology. Cold wall technology is the traditional method. Here, an array of tungsten or halogen lamps heats the wafer through radiation. This process brings the wafer up to the requires temperature within a few seconds. However, the wafer is not in thermal equilibrium with the chamber itself or the lamp, so this can lead to non-uniformities in the anneal process. Hot wall technology is the newer method. Here, heating elements like silicon carbide radiate blackbody heat to the wafer through convection and conduction. This method leads to a more uniform temperature profile, which means a more uniform anneal process across the wafer.

Figure 2. Rapid thermal processing hardware

Figure 2 shows examples of rapid thermal processing hardware. The image on the left shows a rapid thermal processing system from the exterior. The image on the right shows the RTP chamber, with a wafer in the system. While RTP is a relatively new technique, process engineers now use it for a wide variety of processing steps in modern semiconductor processing. The precise control makes it invaluable for placement of dopant atoms, alloying of materials, curing of low-k dielectrics, and annealing steps.

Ask the Experts

This time, I thought we might answer a question posted to the Failure Analysis Group on LinkedIn:

Q: Recently we received a PCBA (printed circuit board assembly) with a detached BGA (ball grid array). The pads look black in an optical microscope, so we refer to this as the "Black Pad" issue. The analysis results revealed mud crack symptoms and severe corrosion activities on the Nickel layer of the PCB pads. What might be causing this?

A: You might want to see if you can determine the phosphorus content present on the surface of the surface of the pads. The black discoloration definitely sounds like corrosion, but it would be good to know what the other element in the corrosion product is. Excess phosphorus on the pads can cause this type of problem.

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Chris Henderson of Semitracks will speak at the 2013

IEEE Conference on Reliability Science for Advanced Materials and Devices

Sunday, February 24 – 25, 2013

Colorado School of Mines • Golden, Colorado

http://csmspace.com/events/rsamd

Spotlight on our Courses: Advanced Thermal Management and Packaging Materials

Instructor: Dr. Carl Zweben

Thermal management issues are receiving more a more attention. These range from the high-profile thermal issues with the lithium-ion batteries in the Boeing 787, down to thermal issues at the chip level, like the ones seen in the past with the Nvidia graphics chip. As the electronics industry grapples with techniques to "get the heat out," there are actually a number of workable solutions for many scenarios. This course covers these topics for the chip, package and board level thermal management scenarios. If you are interested in attending this course, or if you are interested in having this done as an in-house course for your staff, please feel free to contact us at (505) 858-0454, or at info@semitracks.com.

COURSE OVERVIEW

The electronic and photonic (*e.g.,* laser diodes, LEDs, displays, etc.) industries face critical heat dissipation, thermal stress, weight and size problems. In the aerospace industry, this issue is called SWaP (size, weight and power). In response to the significant deficiencies of traditional thermal management materials, there are an increasing number of advanced materials. They have low coefficient of thermal expansions (CTEs), low-densities, and thermal conductivities up to 1700 W/m-K. Some are now low cost; others have the potential to be low cost in high-volume. They are being used in every packaging level, from module to enclosure. Production applications include numerous commercial and aerospace/defense electronic and photonic systems, including handsets, servers, laptops, cellular telephone base stations, electric and hybrid vehicles, power modules, high-power RF, phased array antennas, avionics, vetronics, telecommunications, laser diodes, LEDs, and displays, among many others. To illustrate the advantages, one IGBT manufacturer reports that replacing copper base plates with one advanced material eliminates solder joint failure ("The failure mechanism does not exist any longer"). Advanced thermal materials are also being used to reduce surface temperatures of consumer products. ***Advanced Thermal Management and Packaging Materials*** is a two-day course that covers the increasing number of advanced thermal management materials and provides an in-depth discussion of properties, manufacturing processes, applications, cost, lessons learned, typical development programs, and future directions. Traditional materials are discussed for reference. The focus is on materials used for heat spreaders, heat sinks, substrates, printed circuit boards (PCBs), enclosures/chassis, etc., but we also consider emerging advanced thermal interface materials (TIMs). Participants are invited to bring their thermal management problems for discussion. This course is designed for every manager, engineer, and technician concerned with packaging materials, using semiconductor components, or supplying materials to the industry.

What Will I Learn By Taking This Class?

At the end of this seminar, participants will be able to determine which materials will be best for a given application and will know how to test them, develop analytical models using them, and implement them in the product.

1. **Survey of Traditional Thermal Management and Packaging Materials.** Participants learn the thermal and mechanical properties of both traditional packaging materials. Many engineers are only familiar with copper and aluminum. This segment provides a frame of reference for new materials.
2. **Overview of Composite Materials.** Participants learn the characteristics of four important classes of materials systems being used in the industry today: metal matrix composites, polymer matrix composites, carbon matrix composites and ceramic matrix composites.

3. **Advanced Thermal Materials Properties.** Participants learn the thermal and mechanical properties of advanced carbon-based and composite materials.
4. **Manufacturing Methods.** Participants learn the manufacturing methods behind these materials
5. **Cost Issues.** Participants learn the issues affecting component and system cost.
6. **Applications.** Participants learn the electronic and photonic applications of the materials for both the system and package levels.
7. **Lessons Learned.** Learn from the mistakes of others.
8. **Future Directions.** We look at likely future developments.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the advantages and disadvantages of advanced materials, and how they compare to traditional ones.
2. Participants will be able to identify appropriate materials for a wide variety of applications.
3. The seminar will identify key thermal and mechanical properties of both traditional and advanced materials.
4. The seminar offers the opportunity to ask specific questions to one of the world's leading experts on thermal management materials.
5. Participants will be able to understand manufacturing methods for advanced and traditional materials.
6. Participants will be able to understand the costs and implementation issues associated with a variety of materials.
7. Learn from the mistakes of others.
8. Future directions.

COURSE OUTLINE

1. Introduction
    a. Thermal Management Problem and Packaging Problems
    b. Examples of costly (e.g. $1 billion) thermal problems
    c. Solutions
    d. Packaging Functions
    e. Overview of packaging levels from module to enclosure (chassis)
    f. Key Trends
    g. Packaging Design Drivers
    h. Material Requirements
    i. What's wrong with Traditional Materials?
    j. Classes of Advanced Materials: Composites, Carbonaceous (Carbon-Based)
    k. History of Composites in Packaging
    l. Example: The Most Successful Advanced Thermal Management Material - Al/SiC

2. Overview of Composite Materials
   a. Definitions
   b. Terminology
   c. Classes of Composites
   d. Types of Reinforcements
   e. Thermally Conductive Carbon Fibers
   f. Types of Laminates
   g. Thermally Conductive Carbonaceous (Carbon-Based) Materials
   h. Discontinuous vs. Continuous Reinforcements
3. Material Property and Test Method Issues
   a. Examples of Variability in Reported Material Properties
   b. Sources of Reported Property Variability
4. Properties of Traditional Packaging Materials
   a. Semiconductors
   b. Ceramic Substrates
   c. Monolithic Metals
   d. Polymers
   e. Metal/Metal Composites and Alloys
   f Multimaterial Laminates
   g. Printed Circuit Board Materials
   h. Brief Overview of Thermal Interface Material Properties
   i. Brief Overview of Solder Properties
5. Properties of Advanced Materials
   a. Overview of Advanced Materials
   b. Advanced Material Payoffs
   c. Disadvantages of Advanced Materials
   d. Electromagnetic Interference Shielding and Emissions
   e. Abbreviations
   f. Monolithic Carbonaceous (Carbon-Based) Materials
   g. Polymer Matrix Composites (PMCs)
   h. Advanced Thermal Interface Materials
   i. Metal Matrix Composites (MMCs) and Advanced Alloys-Composites
   j. Advanced Multimaterial Laminates
   k. Carbon Matrix Composites (CAMCs)
   l. Ceramic Matrix Composites (CMCs)
6. Manufacturing Methods for Composite Materials
   a. Overview of Composite Manufacturing Processes
   b. Thermoset Polymer Matrix Composites
   c. Thermoplastic Polymer Matrix Composites
   d. Metal Matrix Composites
   e. Carbon Matrix Composites
   f. Ceramic Matrix Composites

7. Using Composites to Improve Manufacturing Yield
    a. Warping and Thermal Stresses
    b. Tailoring Composite Properties to Reduce Warping and Thermal Stresses
    c. Example: Using Composites Saved USD $60 Million
8. Cost Considerations
    a. General Considerations
    b. Reinforcement Costs
    c Composite Material Costs
9. Applications
    a. Overview of packaging levels from module to enclosure (chassis)
    b. System Applications
    c. Component Applications
10. Typical Development Plan for Introduction of Advanced Materials in Products
    a. Establishing Requirements
    b. Selection of Candidate Materials
    c. Material Property Database
    d. Design Trades
    e. Process Development
    f. Prototype Fabrication
    g. Qualification
    h. Production
11. Lessons Learned
12. Future Trends
    a. General Trends
    b. Monolithic Materials
    c. Reinforcements, Including Carbon Nanotubes and Nanofibers, Graphite Platelets
    d. Matrix Materials
    e. Polymer Matrix Composites
    f. Metal Matrix Composites
    g. Carbon Matrix Composites
    h. Ceramic Matrix Composites
    i. Solders
    j. High-Performance Thermal Interface Materials
    k. Smart Composites and Multifunctional Materials
    l. Processes
    m. Applications
13. Summary and Conclusions
14. Open Discussion

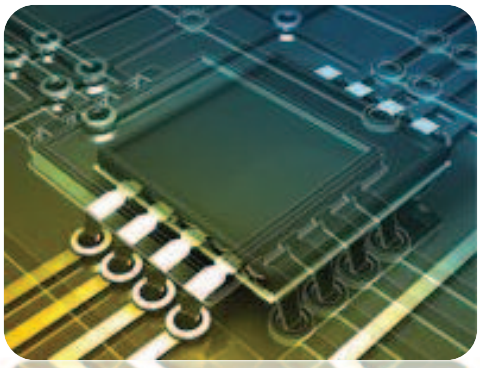
Instructional Strategy

By using a combination of instruction by lecture, problem solving and question/answer sessions, participants will learn practical approaches to choosing the appropriate materials. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. Our instructors are internationally recognized experts in their fields and have years of experience (both current and relevant). The course notes offer hundreds of pages of reference material the participants can use back at their daily activities.

Instructor Profile

Dr. Carl Zweben

Dr. Carl Zweben, now an independent consultant, directed development and application of advanced thermal management and packaging materials for over 30 years. He was formerly Advanced Technology Manager and Division Fellow at GE Astro Space, where he directed the Composites Center of Excellence. His group developed and applied advanced thermal management materials and low-CTE printed circuit boards. It was the first to use Al/SiC, which is now well established in microelectronic and photonic packaging. Other affiliations have included Du Pont, where he worked on low-CTE aramid printed circuit board materials, Jet Propulsion Laboratory, the Georgia Institute of Technology National Science Foundation Packaging Research Center and Materials Science Corporation. Dr. Zweben was the first, and one of only two winners of both the GE One-in-a-Thousand and Engineer-of-the-Year awards. He is a Life Fellow of ASME, a Fellow of ASM and SAMPE, an Associate Fellow of AIAA, and has been a Distinguished Lecturer for AIAA and ASME. He has published and lectured widely on advanced thermal management and packaging materials, and has directed and presented over 250 short courses in North America, Europe and Asia.



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Wafer Level Chip Scale Packaging
February 25 – 26, 2013 (Mon – Tue)
Penang, Malaysia

Copper Pillar Bumping
February 28 – March 1, 2013 (Thur – Fri)
Penang, Malaysia

Failure and Yield Analysis
March 18 – 21, 2013 (Mon – Thurs)
San Jose, California

Wafer Fab Processing
March 26, 2013 (Tues)
San Jose, California

Fundamentals of Yield (co-sponsored by SEMI)
March 27, 2013 (Wed)
San Jose, California

Semiconductor Reliability
April 3 – 5, 2013 (Wed – Fri)
San Jose, California

Failure and Yield Analysis
April 8 – 11, 2013 (Mon – Thurs)
Penang, Malaysia

Photovoltaics Reliability (co-sponsored by SEMI)
April 18, 2013 (Thurs)
San Jose, California

Advanced Thermal Management and Packaging Materials
April 22 – 23, 2013 (Mon – Tues)
Philadelphia, Pennsylvania

Upcoming Webinars

(Click on each item for details)

An Overview of the Semitracks Online Training System
February 7, 2013 (Thu) • 11:00 A.M. EST