

# InfoTracks

Semitracks Monthly Newsletter



## Quartz Disc Storage Systems

By Christopher Henderson

In this short section we will cover a recently developed technology for storing data on a quartz disc.

Researchers demonstrate a high-density five dimensional data storage with ultrafast laser writing. They record a text file by polarization controlled self-assembly from birefringence in a glass disk. They also demonstrate a basic retrieval method as well. In theory, one can store many orders of magnitude more data.

This document will cover several aspects of the quartz disc storage system. This new innovation opens the door for a different type of data storage that has the potential to out perform all current standards. Quartz disc statistics have some interesting properties that set it apart from our current data storage technology. Directly comparing quartz discs to CDs and hard drives, there are several favorable advantages. The process of writing data to these quartz discs requires specialized devices due to the nature of the technology; five physical dimensions are utilized to effect this innovation, but this process may also have limitations that differ from standard read/write technology in computers. Moving forward as a working and new technology, these discs and their associated device processes will require advancement and miniaturization before commercialization can begin. As with all new innovations that have been successfully demonstrated, there is a lot of promise in a future change for computing standards.

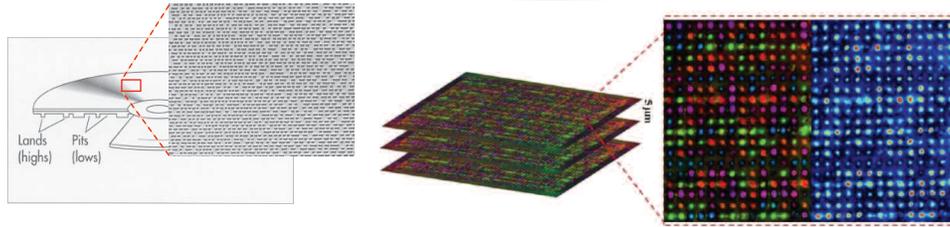
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J. Zang et. al., SPIE 2016

Figure 1. New type of data storage

This technological innovation builds on the specific topic of optical memory from a 1996 Optics Letters paper “Three-dimensional optical storage inside transparent material” by E. N. Glezer et. al. This process incorporates nanostructured quartz crystals that store data in a complex binary sequence. Where CDs have “pit-and-land” structures that define binary data in linear segments for the optical reader to pass over, the quartz crystals form data points with five dimensional orientation alignments among three separate layers. Currently, these data points are read manually with an optical microscope utilizing a quantitative birefringence measurement system (CRi Abrio Macro). In the zoomed image for the quartz crystals, the left half shows slow axis and the right shows retardance distribution.

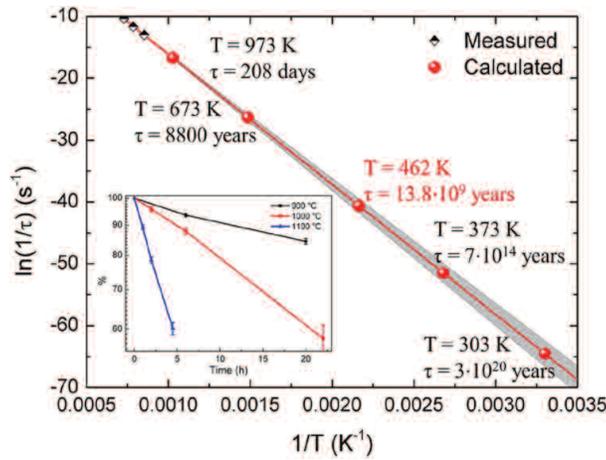


Figure 2. Disc stats

The quartz discs have a storage capacity well above and beyond current CD and DVD discs with 360 Tbs. Vastly different than other storage media, these quartz crystal devices can remain stable at temperatures up to one thousand degrees centigrade. Quartz crystal discs are waterproof, radio wave proof, and should be unaffected by magnetic fields.

Comparing a future with quartz disc storage devices to current devices, some differences are immediately apparent. A major difference is in durability and longevity: CDs are easy to scratch and damage, and hard drives can have catastrophic failures from any number of issues. Quartz is durable having a hardness of seven on Mohs scale, which is harder than steel nails. Hard drives have a tendency to

fail for a number of reasons and corrupt its storage, not to mention the hardware being susceptible to magnetic fields. CDs and hard drives have low thermal tolerances. While Moore's Law pertains to transistors on ICs (1965), Intel's own R&D is working to integrate single crystal nanostructures with semiconductor III-V materials to advance modern technology.

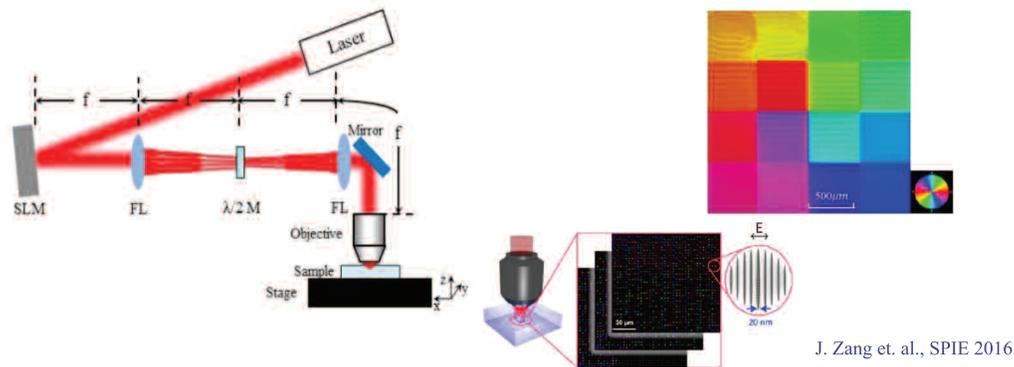
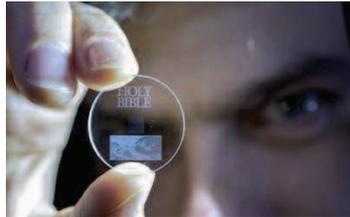


Figure 3. Process device

Using a femtosecond "PHAROS" laser (manufactured by Light Conversion Ltd), the quartz crystals are "written" to the disc. The spatial light modulator (SLM) is utilized with the beam intensity distribution at the focal plane, splitting the incident light into 256 beams. This creates a hologram that is then reimaged through the four 'f' optical system on the back pupil of the objective. Between the two Fourier lenses, a half-wave plate matrix is incorporated for motion free polarization control, which is imprinted by the laser nanostructuring of fused silica. The laser is then focused with a 1.2 NA water immersion microscope objective 140  $\mu\text{m}$  below the surface of the sample. The image on the top right in Figure 3 is the color-coded slow axis orientation of the half wave-plates matrix imprinted in silica glass.

The specific construction of the discs and then writing of the data on these discs may have unique technological limitations. The data is "written" into the crystals in five different dimensions: X,Y,Z and then crystal size and crystal orientation. Once the crystals are set, will this prevent realignment of the crystals, making each disc a read-only medium? This technology will require specialized devices, just like our current disc drives require specific mechanical readers, drive bays, and interface slots.



Southampton, Feb 2016

Figure 4.

This technology already works, and has been used to “write” several quartz discs with some very monumental and historically significant documents. Before it can be commercially available to the world, the technology will need to make several more advancements, including miniaturization for home and corporate use. Even if the discs are not re-writable, an archive of data will still need a device to read the discs and be small enough or portable enough for common office space use.

For further reading, listed below are two references related to the technology.

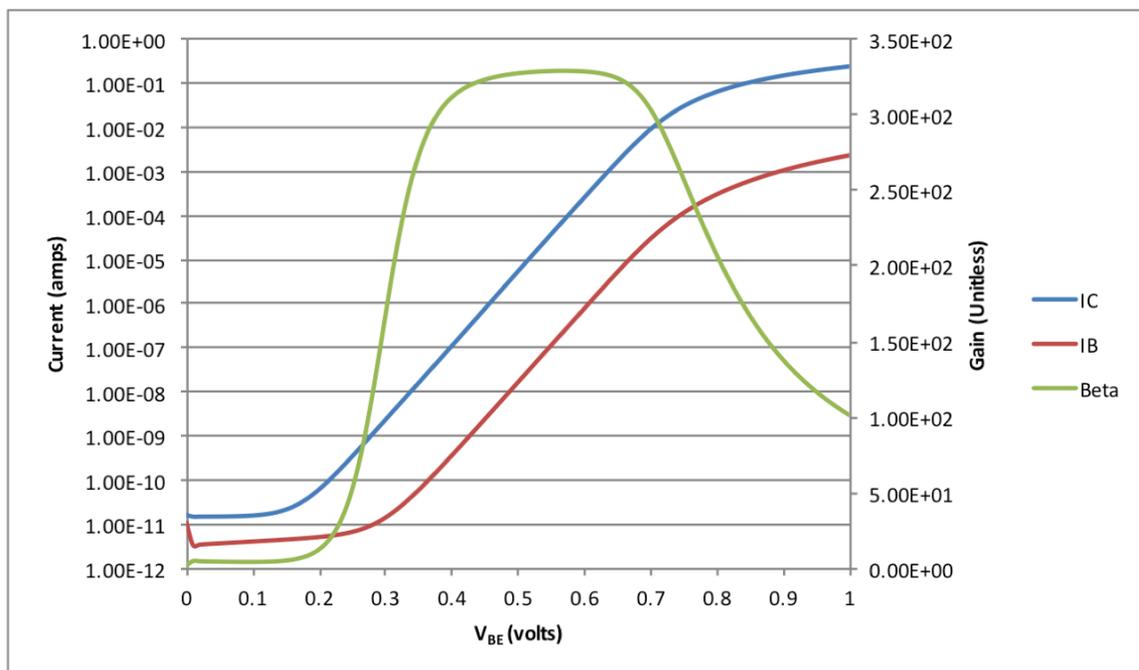
- 1) Jingly Zang, et. al., “Eternal 5D data storage by ultrafast laser writing in glass”, International Society for Optical Engineering Conference, paper 9736-29, February 2016
- 2) University of Southampton, “Eternal 5D data storage could record the history of humankind,” *News and Events/Latest News*, 18 February 2016 Web.

<http://www.southampton.ac.uk/news/2016/02/5d-data-storage-update.page>

## Technical Tidbit

### Gummel Plot

In this article, we will discuss the Gummel Plot. The Gummel Plot shows the current of the base and collector as a function of the base-emitter voltage ( $V_{BE}$ ) of a bipolar junction transistor on a single plot. Quite often the plot will include a secondary axis that shows beta as a function of  $V_{BE}$  as well. The Gummel Plot was named after Hermann Gummel, who also helped to develop the Gummel-Poon model of the transistor that engineers use in SPICE simulations.



The Gummel plot, with beta plotted as a function of  $V_{BE}$ , shows how the gain of the transistor varies with base-emitter voltage. Notice the the gain peaks around a  $V_{BE}$  of 0.5 – 0.6V. Above that value, the gain rolls off because of high level injection. The electron concentration becomes greater than the hole concentration in the base. Below that value, the gain rolls off because of electron-hole recombination in the emitter. The Gummel plot can be used to determine the base Gummel number, or GB. GB is simply the slope of the  $I_C$  curve as a function of  $V_{BE}$ . For the transistor in this graph, the slope is approximately 60mV/decade.



## Ask the Experts

**Q: What is the difference between verification and validation?**

**A:** Although some companies will use the terms interchangeably, the best way to think of these two terms, and to differentiate between the two, is to think of verification as being a “pre-silicon” activity, and validation being a “post-silicon” activity. Verification involves verifying that the design code and layout results conform with the original specifications. This involves design tools and designers will sometimes refer to this activity as formal verification. Validation involves running completed wafers or packaged parts through an extensive set of test and characterization steps, involving Automated Test Equipment and potentially specialized test platforms that simulate the customer’s circuitry or application environment.

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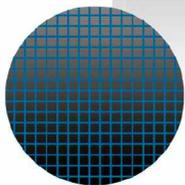
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## Spotlight: Advanced CMOS/FinFET Fabrication

### OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" Advanced CMOS/FinFET Fabrication is a one-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

### WHAT WILL I LEARN BY TAKING THIS CLASS

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs and FD-SOI are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including ion implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.
2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.
3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.
4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

### COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of SOI technology and the technical issues.
2. Participants will understand how Hi-K/Metal Gate devices are manufactured.
3. Participants will also understand how FinFET devices are manufactured.
4. The seminar provides a look into the latest challenges with copper metallization and Low-k dielectrics.

5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.
6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.
7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.
8. Finally, the participants see a comparison between FD-SOI (the leading alternative) and FinFETs.

## COURSE OUTLINE

1. Advanced CMOS Fabrication – Introduction
2. Front End Of Line (FEOL) Processing
  - a. SOI and FD-SOI
  - b. Ion Implantation and Rapid Thermal Annealing
  - c. Pulsed Plasma Doping
  - d. Hi-K/Metal Gates
  - e. Processing Issues
    - i. Lithography
    - ii. Etch
    - iii. Metrology
3. Back End Of Line (BEOL) Processing
  - a. Introduction and Performance Issues
  - b. Copper
    - i. Deposition Methods
    - ii. Liners
    - iii. Capping Materials
    - iv. Damascene Processing Steps
  - c. Lo-k Dielectrics
    - i. Materials
    - ii. Processing Methods
  - d. Reliability Issues
4. FinFET Manufacturing Overview
  - a. Substrates
    - i. Bulk
    - ii. SOI
  - b. FinFET Types
  - c. Process Sequence
  - d. Processing Issues
    - i. Lithography
    - . Etch
    - . Metrology

5. FinFET Reliability
  - a. Defect density issues
  - b. Gate Stack
  - c. Transistor Reliability (BTI and Hot Carriers)
  - d. Heat dissipation issues
  - e. Failure analysis challenges
6. Future Directions for FinFETs
  - a. Comparison of FD-SOI and FinFETs—Are FinFETs a better choice?
  - b. Scaling

# GSEF

Global Semiconductor and Electronics Forum



## 2017 Global Semiconductor and Electronics Forum

Gsf Gef

March 8-10, 2017  
Hong Kong, China

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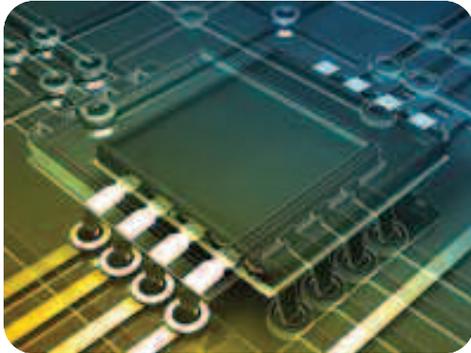
Registration is available at [www.arena-international.com/gsef](http://www.arena-international.com/gsef)

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**Chris Henderson**

Chris would be happy to meet with you and discuss any training needs you have. Contact him at [henderson@semitracks.com](mailto:henderson@semitracks.com) during the forum!




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## Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us ([info@semitracks.com](mailto:info@semitracks.com)).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email ([jeremy.henderson@semitracks.com](mailto:jeremy.henderson@semitracks.com)).

We are always looking for ways to enhance our courses and educational materials.

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*To post, read, or answer a question, visit our [forums](#).  
We look forward to hearing from you!*

## Upcoming Courses

(Click on each item for details)

### Failure and Yield Analysis

Jan 30 – Feb 2, 2017 (Mon – Thur)  
Portland, Oregon, USA

### Advanced CMOS/FinFET Fabrication

Feb 6, 2017 (Mon)  
Portland, Oregon, USA

### Semiconductor Statistics

Feb 7 – 8, 2017 (Tue – Wed)  
Portland, Oregon, USA

### Defect Based Testing

May 3 – 4, 2017 (Wed – Thur)  
Munich, Germany

### Failure and Yield Analysis

May 8 – 11, 2017 (Mon – Thur)  
Munich, Germany

### Semiconductor Reliability and Qualification

May 15 – 18, 2017 (Mon – Thur)  
Munich, Germany

### Semiconductor Statistics

May 22 – 23, 2017 (Mon – Tue)  
Munich, Germany