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An Overview of BiCMOS

By Christopher Henderson

Many engineers consider BiCMOS to be a niche technology, but it has a number of practical advantages for electronics applications. In this article, we will discuss BiCMOS devices. BiCMOS is a technology that combines both bipolar and CMOS transistors on to the same chip.

One reason why engineers consider BiCMOS when designing circuits for certain applications is noise. Precision circuits require large signal to noise ratios. Flicker, or 1/f noise, can be an issue down to less than 200 Hz. BiCMOS is also key to handling oscillator phase noise, which influences mixer noise. Engineers also use BiCMOS to improve oscillator purity and clutter rejection. BiCMOS can also reduce low jitter noise in high-speed digital applications, for example, clock recovery in fiber communication. This requires higher supply voltages, but the trend is toward lower voltages. In BiCMOS though, there is a lower noise bandwidth. It is approximately one nanovolt per root hertz in BiCMOS, but some ten times higher in conventional CMOS circuits. BiCMOS also provides superior mismatch capabilities in transistors. Engineers can currently design transistors that have approximately three times better mismatch characteristics in BiCMOS than they can in conventional CMOS.

Another advantage for BiCMOS is its current drive. Bipolar transistors provide a larger drive per unit area than standard

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CMOS transistors. Engineers can use this characteristic to create emitter-coupled logic for critical high-speed circuits, and then use CMOS for lower-power, lower-speed logic functions. The bipolar transistors in a BiCMOS circuit exhibit a higher transconductance than with CMOS. This leads to superior amplification properties. Bipolar transistors also exhibit higher cutoff frequencies than CMOS transistors, even when engineers make CMOS transistors small. Another advantage is an improved Early voltage. In a CMOS circuit, transistors with high drive capability exhibit a small Early voltage, which leads to poor transistor properties for some analog applications. Bipolar transistors maintain a larger Early voltage. Still other BiCMOS advantages include improved band-gap reference circuits, and a larger array of electrostatic discharge options.

Some examples of BiCMOS applications include radio frequency and mixed-signal applications like low noise amplifiers and mixers. We show an example of a low noise amplifier in Figure 1 below. Other BiCMOS functions include voltage controlled oscillators, and a variety of high-speed amplifiers, including variable gain and programmable gain amplifiers. Other major class of components for which BiCMOS can provide better performance are Analog-to-Digital, and Digital-to-Analog circuits. High-speed Analog-to-Digital converters in particular benefit from the strengths of BiCMOS. Yet another category is the disk drive pre-amplifier. Engineers can make the readers and writers faster and more accurate through the use of BiCMOS.

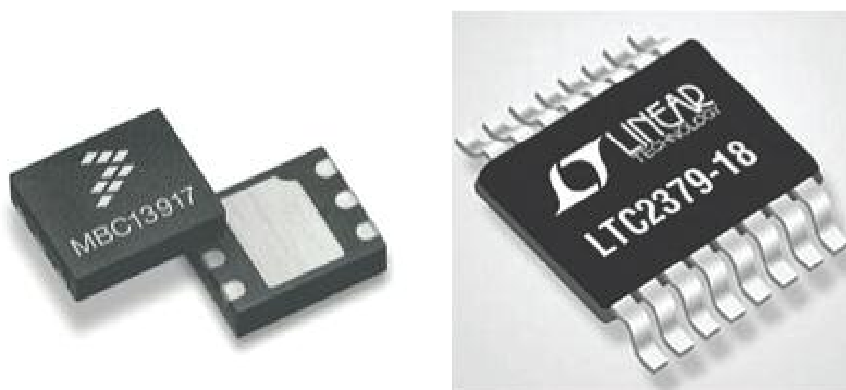


Figure 1. The image on the left is courtesy of Freescale Semiconductor; the image on the right is courtesy Linear Technology.

Figure 2 shows a schematic cross-section of a notional BiCMOS technology. Basically, this technology combines bipolar and CMOS transistors on the same chip. The CMOS transistors appear on the left, and the bipolar transistors on the right. As we'll discuss later on, some of the features of the CMOS and bipolar transistors can be defined simultaneously, while other features require additional processing steps. This makes BiCMOS more complex from a processing standpoint, so the gains in performance need to be more significant than the cost increase.

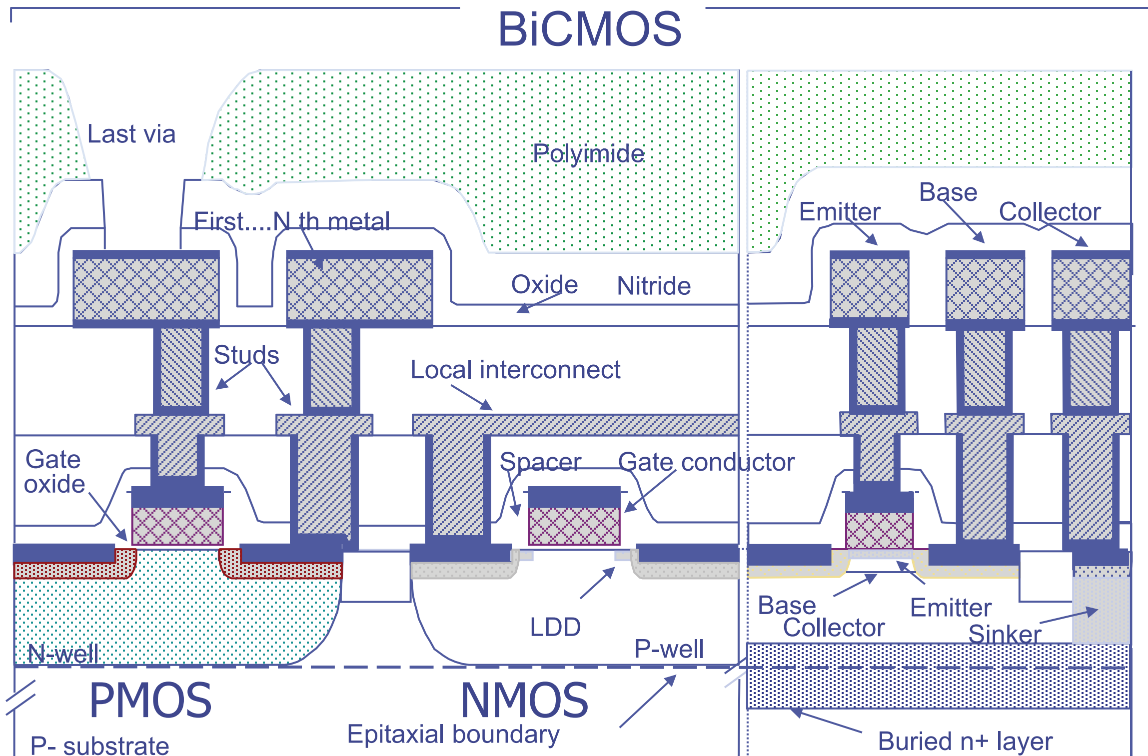


Figure 2. Cross-section of a typical BiCMOS technology.

Figure 3 presents a simplified flow for a BiCMOS process. This approach groups related processes into modules. We begin with the initial wafer, followed by the buried layers and epitaxial growth. Next, we define the isolation regions for the transistors, followed by the sinkers to make connections to the buried collector structures. We define and create the wells, and then define and grow/deposit the gate stack. We then define and implant the base regions, followed by the emitter regions, and then the precision resistors. Next we define the source and drain regions in the CMOS transistors, followed by silicidation for improved performance. We then implement the precision capacitors as metal-insulator-metal structures, and end by forming the contacts, and creating the metal routing and dielectric isolation for connecting the transistors to one another. If done properly, one can implement the CMOS structures with 14 to 16 mask steps, and the analog/BiCMOS/bipolar transistors in 14 to 16 mask steps as well.

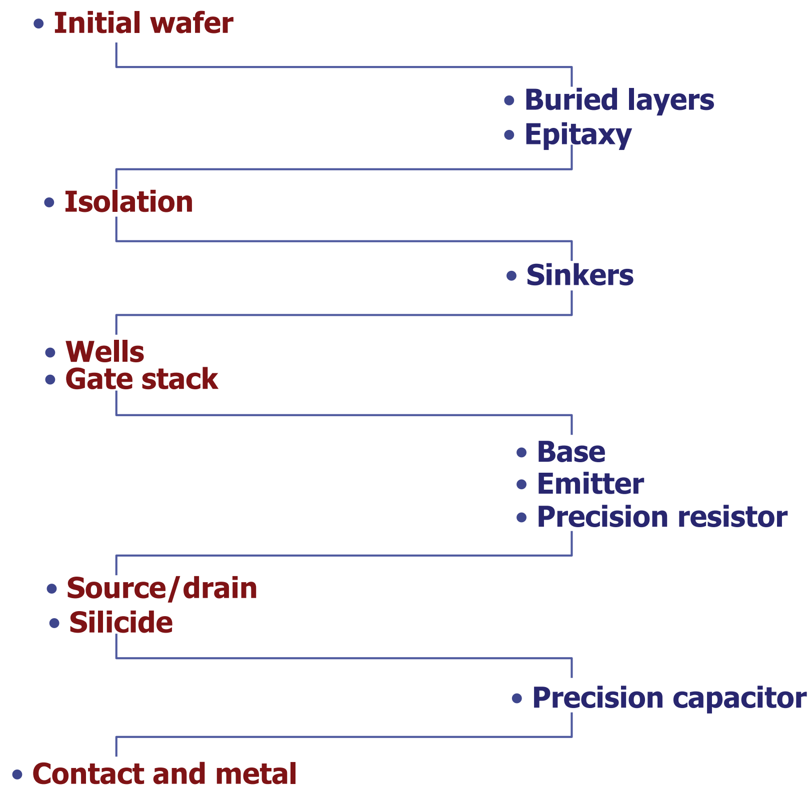


Figure 3. Simplified process flow for a BiCMOS process.

Let's now describe the process modules in a bit more detail. BiCMOS typically uses a high-resistivity p-type wafer. This allows for a buried n+ layer for vertical npn transistors like we described in other sections. These buried layers are used to reduce the collector resistances. This method allows for lower resistance while maintaining higher breakdown voltages for applications that require higher voltages. BiCMOS wafers use an epitaxial layer on top of the p-substrate. This not only improves the CMOS transistors, but also ensures that one can create a larger vertical distance between the buried layers and the active areas. The alternative would be to attempt to deeply implant to create a buried layer, which would require expensive high-energy ion implanters and extensive annealing. Isolation is a key module for BiCMOS devices. Engineers use shallow trench isolation to separate the CMOS source and drain regions and the bipolar transistors, and deep trench isolation to separate the bipolar collectors and reduce the parasitic capacitance. BiCMOS also requires vertical isolation for npn and pnp transistors, and it can eliminate latch-up as well as reduce parasitic capacitances. Finally, dielectric isolation, rather than junction isolation will allow higher operating voltages and reduced parasitic capacitances.

BiCMOS devices commonly employ sinkers, or deep implants that connect to the buried layer. This is the next major module and these reduce the collector resistance. The next module is well implant. The

well implant profile tailors the threshold voltage, stops the punch-through phenomenon, and prevents channeling under the shallow trench isolation. The gate stack module covers the gate formation process for the CMOS transistors. It consists of the gate oxide, the gate conductor, and in some applications, the top insulator. The gate oxide layer is the most sensitive layer to defects and variations, so this step of the process is critical. Engineers prepare the surface of the silicon prior to gate oxidation. After gate oxidation, polysilicon deposition is critical to ensure working MOS transistors. The next major module is the base module. Engineers grow the npn and pnp bases through epitaxy; they can be in-situ doped or implanted. They can use selective or non-selective epitaxial growth. In a non-selective epitaxial growth module, engineers grow a single crystal layer over the silicon, and polycrystalline silicon over polysilicon or the insulators. Non-selective epitaxial growth is more common, and it also allows engineers to form contacts over the field oxide. Control of the base thickness and uniformity is important. Engineers will also use this module to deposit silicon-germanium, or silicon-germanium-carbon, which we discuss in a related section close by.

Next is the emitter module. Process engineers typically form the emitter region by diffusing arsenic or boron from the polysilicon material. The surface preparation prior to polysilicon deposition is critical, along with control of the emitter junction depth. The next module is the precision resistor module. This is required for some analog applications that require accurate-valued resistors. The temperature and voltage coefficients are key, as well as low parasitic capacitance. Engineers create lower accuracy resistors by tailoring dopants in polysilicon layers, and higher accuracy resistors by using materials like nickel-chromium alloys, or nichrome. The next module is the source-drain module. This also includes the lightly doped drain regions in the MOS transistors. The gate and the contacts to the wells, collectors, and bases can be doped at the same time as the source and drain. We discuss several variants of doping techniques in our online training web site. Here, the main objective is to reduce the series resistance, overlap capacitance, electrical field, and leakage. In particular, reducing the electric field will reduce the effect of hot carrier damage.

Next comes the silicide module. Engineers form silicide by depositing a refractory metal like titanium, cobalt, or platinum over the polysilicon and annealing in steps. This serves to reduce the series resistance in the gate, source, and drain regions, and form landing pads for contacts on the silicon. Next is the precision capacitor. Like the resistor, design engineers the precision capacitor in a number of analog applications like operational amplifiers. The voltage and temperature coefficients, as well as the parasitic resistances and capacitances are key. Process engineers form these capacitors by depositing a dielectric

between two metal or heavily doped polysilicon layers. The final module is the contacts and metal module. Process engineers closely monitor minimum contact size, the current carrying capability of the metal and its resistance to electromigration, its electrical resistance, and the parasitic capacitance of the metal to adjacent metal and active structures.

Finally, let's spend a minute on scaling. While scaling is a prevalent topic in in CMOS, it is not discussed as much when it comes to BiCMOS. In general, operating voltages limit the amount of scaling that can occur. Lateral scaling will reduce the minimum feature size, making lithography and processing more difficult, although there can be an improvement in alignment and overlay tolerances that would be inherited from CMOS scaling. There is a reduced thermal budget, and a reduced operating voltage. This would be limited by signal-to-noise ratios and other circuit requirements. Process engineers also need to increase the dopant concentrations to suppress punch-though in the circuit, but there is a limit to what they can do because of parasitic capacitance increases. Vertical scaling can reduce the base width. This improves the transistor speed, but degrades the Early voltage and the breakdown voltage. Scaling reduces the emitter depth, which reduces the capacitance, but degrades the current gain and the thermal budget for processing. Some methods to deal with this include alternate doping techniques, which we discuss in a nearby section.

In conclusion, we discussed some of the advantages of BiCMOS circuits over CMOS. The main advantages would be the flexibility to handle higher voltages and improve transistor performance. We discussed some of the analog circuit applications for this technology, including its use in amplifiers, and D-to-A and A-to-D converters. We highlighted the basic process modules and structures for BiCMOS, and showed some cross-sections of typical structures. We discussed the tradeoffs between junction and dielectric isolation for BiCMOS, and we ended with a brief discussion of the scaling issues. BiCMOS, while not a widely used process technology, certainly has its uses for a variety of analog circuit applications, and will continue to be used well into the future.

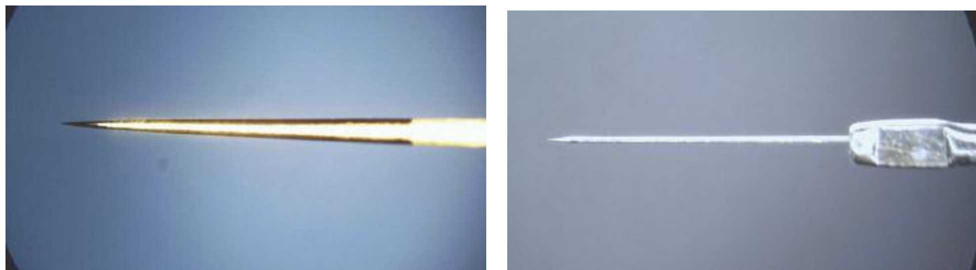
Technical Tidbit

Probes for Microprobing

Occasionally, we have participants ask us which type of probe tip they should buy. It depends on the application, but here are some guidelines.

There are several types of probe materials used for reliability and failure analysis applications. The most common probes are tungsten-based. Tungsten is a hard material that withstands numerous contacts with bond pads. Today, manufacturers are moving toward tungsten alloys. The most popular is tungsten-rhenium. It is less brittle than pure tungsten, giving it better properties for overdrive. Overdrive is the additional pressure applied to the probe tip to help it maintain contact. Tungsten-rhenium still has the hardness necessary for breaking oxide barriers on a probe pad to make good contact. It also has better wear resistance than pure tungsten and works well for high frequency measurements. Another common probe material is beryllium-copper. Beryllium-copper has a lower contact resistance, making it better for high power measurements where resistance can cause heating. They are also useful for measurements that require resolving small changes in resistance, like electromigration testing. Since the tips are softer, they require higher overdrive to make good contact for a long period of time. Therefore, they do not work well for burn-in or life test applications. Another probe material is the conductive fiber probe tip, but it is seldom used in the electronics industry.

Probe tip configurations are normally classified into two categories: standard shank and cat whisker. The "Cat Whisker" probes have a very thin (10 – 50 µm diameter) tip wire that is soldered or otherwise attached to the end of a shank. These tips can bow and straighten when over-driven instead of bending into a fishhook shape. Due to their flexible nature, they do not penetrate oxide and are meant to be used on a clean interconnect surface to insure good contact. They are also useful in applications where one must avoid damage to the circuit. The downside of cat whisker probes is their high resistance.



Standard shank (left) and "cat whisker" (right) probe tips. Images courtesy Pacific Instruments.

Ask the Experts

Q: What is the coefficient of thermal expansion for BT (Bismalemide Triazine)?

A: It is approximately 15 ppm/C in the X and Y directions, and approximately 52 ppm/C in the Z direction. This means that it matches the coefficient of thermal expansion of copper relatively well in the X and Y directions, but not in the Z direction. Plated through holes comprised of copper may be less reliable on a BT substrate. Manufacturers and designers primarily like BT because it can be manufactured with a high glass transition temperature, and it exhibits a low dielectric constant.

Spotlight on our Courses: Reliability and Characterization Challenges for Advanced ICs

As we approach 20nm feature sizes on modern ICs, the Reliability Challenges have become quite difficult. Here at Semitracks we have developed a course that summarizes those challenges for Product, Design, Reliability, and FA engineers that need to understand the issues in a succinct manner. If you are interested in attending this course, or if you are interested in having this course as an in-house course for your staff, please feel free to contact us at (505) 858-0454, or at info@semitracks.com.

OVERVIEW

Semiconductor reliability is at a crossroads. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. Analysis and experimentation must now account not only for material interactions on the die, but also package interactions with the die. This requires knowledge of subjects like: IC processing, new materials and materials science, chemistry, and customer expectations. While reliability levels are at an all-time high level in the industry, rapid changes may quickly cause reliability to deteriorate. Your company needs competent engineers and scientists to help solve these problems. *Reliability and Characterization Challenges for Advanced ICs* is a one-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and characterization. This course is designed for every manager, engineer, and technician who develops new processes, must understand Front End of the Line integration, packaging interactions with the die, and reliability conditions. Engineers involved in reliability, product engineering, wafer manufacturing, assembly, using semiconductor components, or supplying tools to the industry can all benefit from this course.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the transistors, interconnect and dielectric materials used in today's advanced components.
2. Participants will be able to understand the properties of materials and how they affect the IC.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. Participants will be able to identify current reliability issues, how they impact the materials choices for the IC, and how they impact the overall reliability of the IC.

COURSE OUTLINE

Lecture Time: One Day

1. Introduction
    a. Scaling and Its Impact on Reliability
2. Time Dependent Dielectric Breakdown
    a. Energy, Current, Voltage, Electric Field Dependencies
    b. Models
    c. Dealing with Soft Breakdown
    d. Dealing with Hi-κ Materials
    e. Statistical Implications and Circuit Level Modeling
3. Hot Carrier Effects
    a. Physical Behavior
    b. Models for Low, Medium, and High Gate Voltage
    c. P-channel and N-channel Effects
    d. Implications at the Circuit Level
4. Negative Bias Temperature Instability
    a. Mechanism
    b. Fast Measurement Techniques
    c. Reaction-Diffusion Model
    d. New Thinking on Models
    e. Circuit Level Modeling and Behavior
5. Positive Bias Temperature Instability and Hi-κ
    a. Hi-κ Materials Behavior
    b. Fast Measurement Techniques
    c. PBTI Model
    d. Circuit Level Modeling and Behavior

6. Low-κ Materials
    a. What is κ?
    b. Low-κ (organic vs inorganic)
    c. Porosity
    d. Barrier layers (SiN; SiC)
    e. Electrical properties
    f. Mechanical properties
    g. Thermal properties
    h. Thermal and Chemical stability
7. Integration of Cu with Low-κ Materials
    a. Integration options
    b. Effective κ
    c. Patterning
    d. Cleans
    e. Metal deposition
    f. CMP
    g. Packaging
8. Reliability of Cu Interconnects in Low-k Materials
    a. Electromigration
    b. Stress migration
    c. Oxidation
    d. TDDB
    e. Package reliability
    f. Intrinsic vs extrinsic fails
9. Future Reliability Challenges

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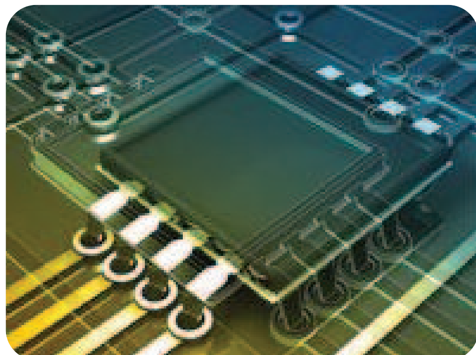

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

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http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

EOS, ESD and How to Differentiate
July 30 – 31, 2012 (Mon – Tue)
Penang, Malaysia

Semiconductor Reliability
August 1 – 3, 2012 (Wed – Fri)
Singapore

Reliability and Characterization Challenges for Advanced Semiconductor Devices
August 14, 2012 (Tue)
San Jose, California

Failure and Yield Analysis
August 27 – 30, 2012 (Mon – Thur)
San Jose, California

Interconnect Process Integration
September 6 – 7, 2012 (Thur – Fri)
Penang, Malaysia

IC Packaging Metallurgy
October 15 – 16, 2012 (Mon – Tue)
Singapore

IC Packaging Metallurgy
October 18 – 19, 2012 (Thur – Fri)
Melaka, Malaysia

Upcoming Webinars

(Click on each item for details)

Acoustic Microscopy
October 8, 2012 (Mon) • 11:00 A.M. EDT

X-Ray Radiography
October 8, 2012 (Mon) • 11:00 A.M. EDT