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YOUR QUARTERLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Transfer Molding

By Christopher Henderson

In this month's Feature Article, we continue our series on Transfer Molding. Transfer Molding is one of the more common steps in semiconductor packaging, and provides protection for the sensitive semiconductor components and packaging interconnect. In this article, we will begin with the electrical properties of mold compounds, and then continue with other important properties, such as their fluidic properties, and their moisture absorption properties.

Let's begin by discussing several important electrical properties associated with epoxy resin mold compounds. The first is resistance. Resistance is a function of a material's resistivity, which in turn is influenced by temperature, pressure, the chemical nature of the materials, stress relief agents, and relative humidity. The second is dielectric constant, or permittivity. This is a property that defines how much charge a material will hold. Typically, a lower dielectric constant is best. A lower dielectric constant provides for better signal integrity. Conversely, not only does a higher dielectric constant material inhibit good signal integrity, but a high dielectric constant material is polar, and will absorb more moisture. A good quality epoxy resin mold compound should also hold these values over a wide range of temperatures, pressures, and humidity levels.

WHAT'S INSIDE?

Want to take control of your learning? See page 9

Upcoming Courses:

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- Failure and Yield Analysis
- Wafer Fab Processing
- Defect Based Testing
- Reliability and Product Qualification
- EOS, ESD and How to Differentiate

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Another important electrical property of epoxy resin mold compound is its dielectric strength, or its ability to withstand voltages without excessive leakage current or a breakout. This depends on the chemical structure of the epoxy resin mold compound, the amount of impurities in it, and the moisture content.

Let's now discuss the fluidic properties of epoxy resin mold compounds. A common test that packaging engineers perform to study the fluidic properties of epoxy resin mold compound is the spiral flow test. The spiral flow test is a measure of the distance that an epoxy resin mold compound will flow under a given set of molding conditions, like mold temperature, transfer pressure, transfer speed, and so forth. The farther the epoxy resin mold compound travels through the spiral flow structure, the lower its viscosity is, given that all other factors are equal. We show an example of the spiral flow structure on the left, and a graph showing the flow distance for several common mold compound formulations in Figure 1.

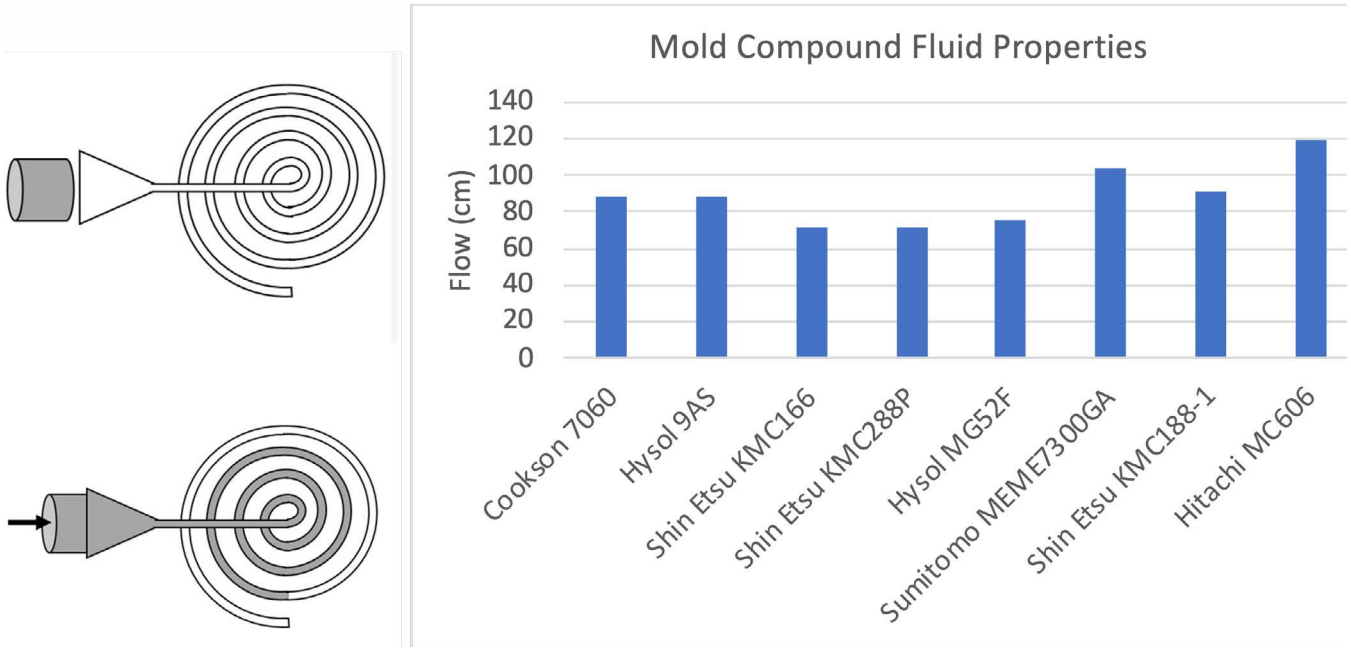


Figure 1- Diagram of spiral flow structure (left) and flow distances for several mold compounds (right).

An important fluidic property of an epoxy resin mold compound is its melt viscosity. Melt viscosity is a measure over time of the resistance of a mold compound to flow when subjected to a given temperature, pressure, and cross-sectional area of confinement. Understanding the melt viscosity of an epoxy resin mold compound is critical when developing optimum mold parameters, so epoxy resin mold compound manufacturers and packaging engineers will often study this property.

Epoxy resin mold compound viscosity changes as a function of the mold injection process. Initially, when the mold injection process starts, the epoxy resin mold compound is a solid tablet. For the following discussion, please refer to the graphs in Figure 2. At this point, the viscosity is quite high, represented by point A on the graph. As the mold compound tablet begins to melt, the viscosity drops significantly, represented by points B and C, eventually reaching a minimum value at point D in the graph. In the range between points C and E, the mold compound flows through the runners and gates from the pot and enters the mold cavities, as shown in the diagram in Figure 2. After the epoxy resin mold compound fills the cavities, the viscosity increases as the resin-hardener system reaches its gelation point, represented by point F. As the epoxy resin mold compound cures, the viscosity continues to increase, represented by point G, reaching a point where the packages can be released from the mold plates. The viscosity increases further as the epoxy resin mold compound reaches its final hardness, represented by point H.

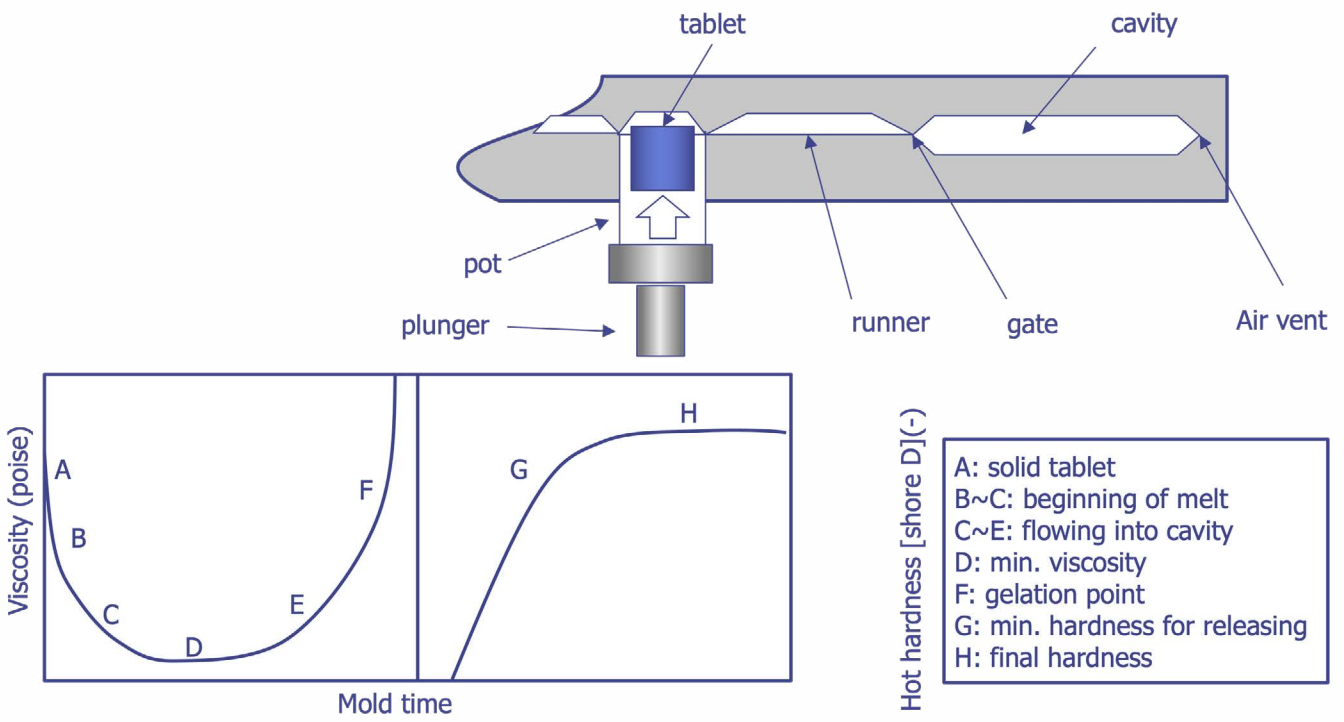


Figure 2- Diagram (upper right) of the mold cavity, and graphs (lower left) showing viscosity changes during the mold process.

The graph in Figure 2 was a notional plot. Figure 3 shows what a viscosity plot looks like for an actual epoxy resin mold compound from Hitachi. Notice that higher curing temperatures allow the viscosity to go lower initially, but increase the viscosity more quickly.

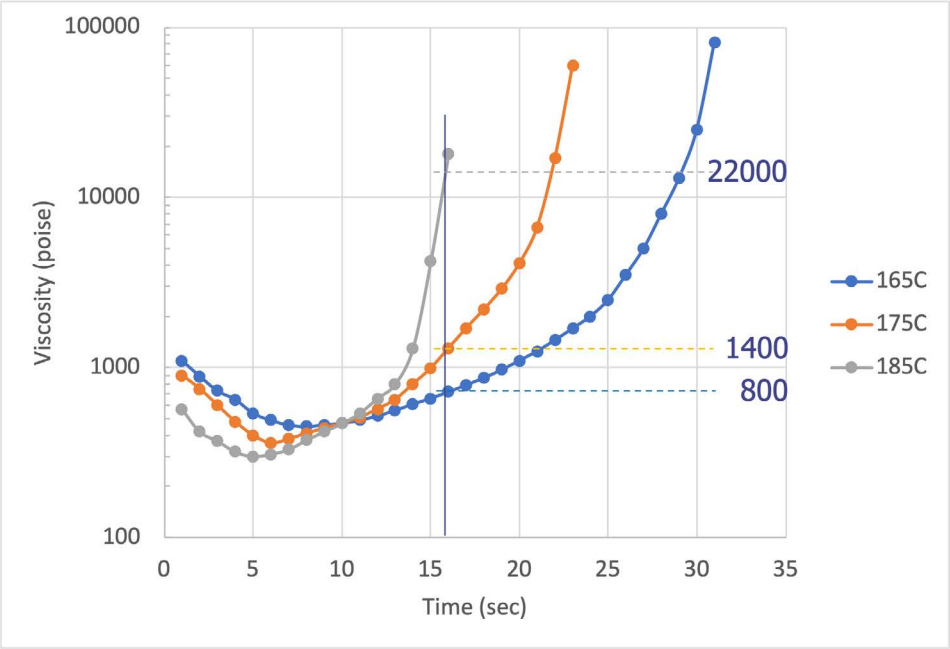


Figure 3- Viscosity plot for a Hitachi mold compound.

Another important fluidic parameter associated with epoxy resin mold compounds is the gelation, or gel time. Gel time is a measure of the time required for an epoxy resin mold compound to cure when subjected to a specific temperature. Packaging engineers typically perform this test on a hot plate. Since there is unevenness of heating and convection properties in epoxy resin mold compounds, this is a very subjective test. However, it is still often used as a relative indicator of cure speed. In Figure 4, we show gel times for eight different epoxy resin mold compound formulations. Notice the gel times range from under 15 seconds to almost 45 seconds, so one can choose an epoxy resin mold compound and tailor it for a specific application.

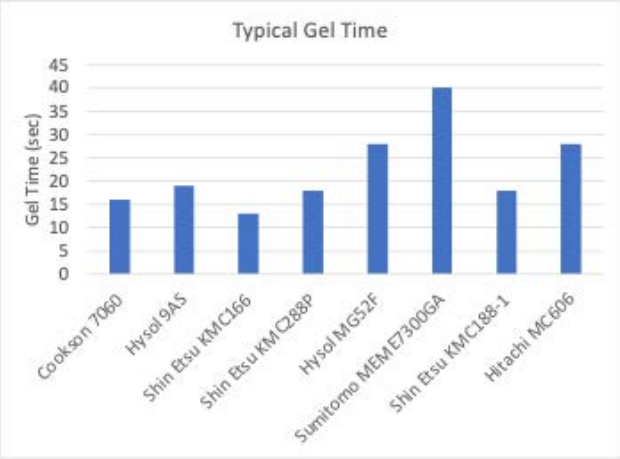


Figure 4- Epoxy mold compound gel times for several mold compounds.

Another important property of mold compound is its resistance to moisture. The amount of moisture within a mold compound affects various properties, including viscosity, void density and kinetics. An optimum moisture level will help reduce viscosity during the mold transfer process. If there is excessive moisture, then voiding can occur. Moisture also affects the cure rate because catalysts within the mold compound are deactivated by moisture. Moisture also accumulates at interfaces, and this accumulation can result in delamination during the soldering process at the next level of electronics assembly. As such, the moisture level in the preform should be strictly controlled. Once the mold compound is cured, the package does offer some amount of protection against moisture, but nonetheless, moisture will slowly penetrate through the cured mold material.

Yet another important property of epoxy resin mold compound is moisture absorption. This property has become increasingly important as packages have become thinner. Thinner packages allow moisture to penetrate more quickly to the die surface. Engineers measure the percent weight gain when a packaged part is exposed to a specific temperature and humidity for a given length of time. This moisture absorption is a key factor in a failure mechanism known as the popcorn mechanism, that can occur during solder reflow. We show the moisture absorption and desorption process graphically in the diagram in Figure 5.

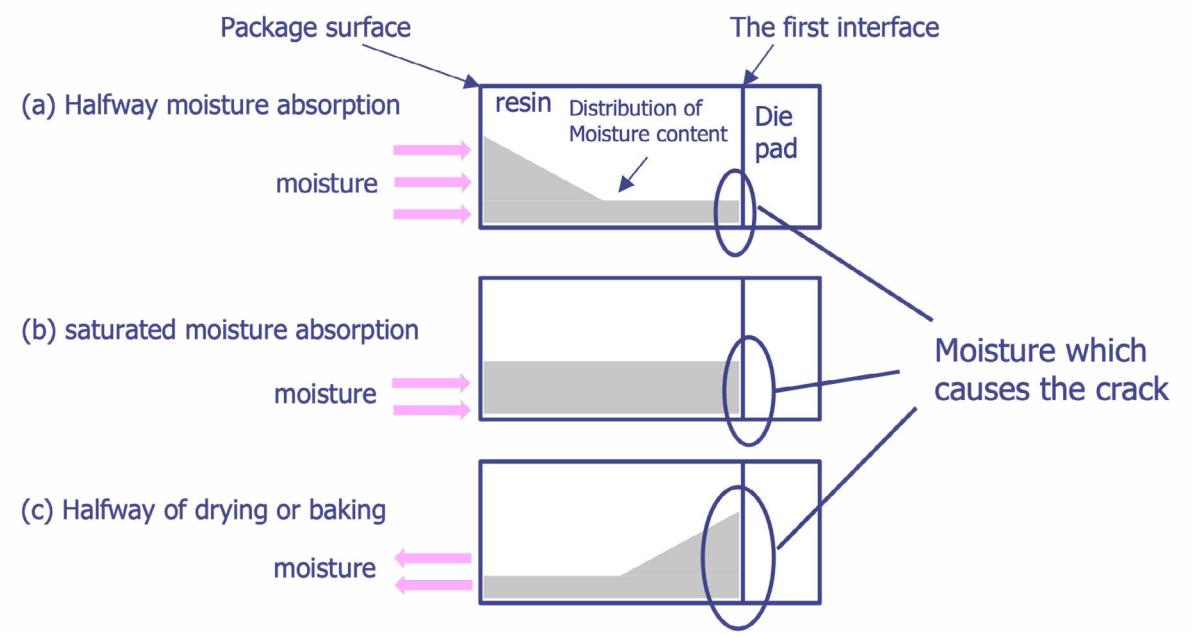


Figure 5- Diagram showing moisture penetration into a mold compound, and subsequent evaporation out of a mold compound.

Figure 6 shows absorption and desorption data for five different epoxy resin mold compound formulations. Notice that the curves rise and fall asymptotically to certain amounts of weight gain, based on the formulation of the epoxy resin mold compound. Each epoxy resin mold compound will have a unique saturation coefficient, and this is reflected in the fraction of weight gain.

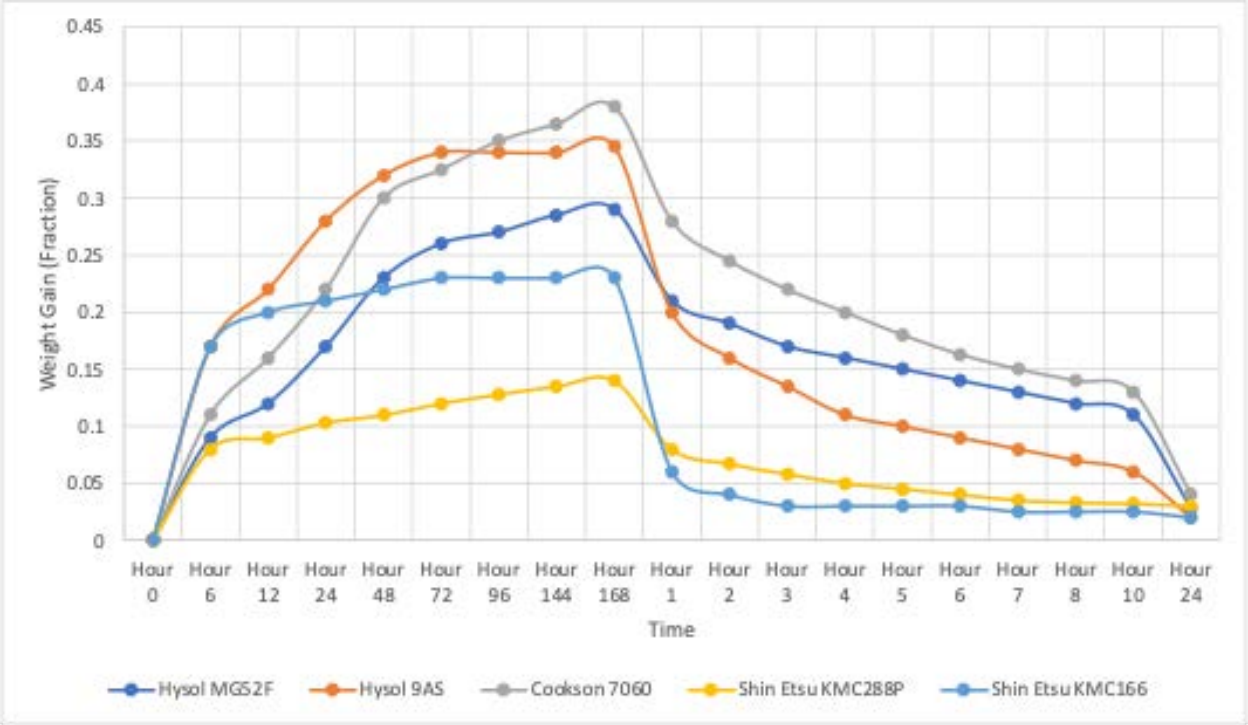


Figure 6- Absorption/Desorption within a mold compound during an 85°C/85% RH test.

Let's now summarize the major chemical and physical characteristics and their impact on the package. Chemical characteristics, like water extraction of mobile ions, or hydrolysable chlorine, impact the reliability of the semiconductor component, affecting corrosion resistance and high temperature storage life. Physical characteristics, like glass transition temperature, Coefficient of Thermal Expansion, flexural modulus, Young's Modulus, mold shrinkage, and water absorption, play an important role in parameters like the cross-linking level, thermal stress, warpage, and Moisture Sensitivity Level, or MSL, capability. Other physical or electrical properties, like volume resistivity and dielectric constant, affect the capacity of the epoxy resin mold compound as an insulator. Finally, flammability will affect the flame retardation characteristics.

In next month's Feature Article, we will continue our discussion of transfer molding by focusing on the equipment used for molding, the process flow, and issues related to the processing.

Technical Tidbit: Anti-Reflective Coatings for Dual Damascene Processes

This month's Technical Tidbit covers Anti-Reflective Coatings (ARCs) for Dual Damascene Processes.

Anti-Reflective Coatings, or ARC layers, are important to aid in the lithography process. These layers help to minimize reflections of light during the lithography process that can interfere with the photoresist patterning process. In a modern dual damascene process, this can be challenging because the ARC layer must fill the via during the trench lithography step.

First, let's provide some background and context. Figure 1 shows the major process integration steps for a copper dual-damascene process with a Silicon-Carbon-Oxygen-Hydrogen molecule, generally referred to as SiCOH, for interlevel dielectric layers. In Step 1, we begin with the via lithography and reactive ion etch down to the silicon carbon nitride hard mask. Next, in Step 2, we perform the lithography to create the trench for the copper metallization. This is where the ARC layer (shown in green) comes into play. We then etch the trench into the SiCOH layer in Step 3. Next, in Step 4, we perform the metal resist strip, followed by the silicon carbon nitride reactive ion etch. This opens a connection path to the metal layer below. Next, in Step 5, we deposit the copper liner and the copper seed layer. We follow this up with the copper electroplating process, followed in Step 6 by chemical mechanical polishing, and then deposition of the capping layer. This process has been pretty much the same since the 130nm node. The one major difference between the 130nm and 14nm nodes, is that the resist mask has been replaced with a SiCN hard mask, like we show in Figure 1.

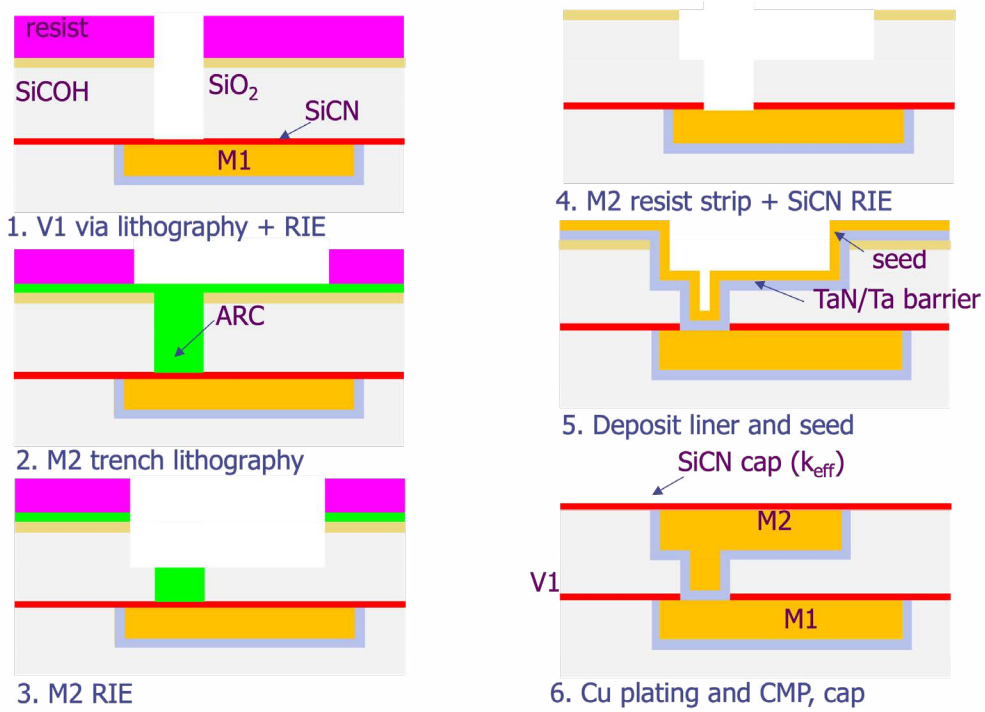


Figure 1- Basic, high-level flow for a dual damascene process. The ARC layer is in green.

ARC layers are often removed after the lithography process, so in that sense, they are sacrificial. The sacrificial ARC layer is formulated to have etch properties similar to those of the SiCOH dielectric layer. In various processes where the Low-k dielectric layer is an inorganic material such as silicon dioxide or Carbon Doped Oxide (CDO), the base material of the sacrificial ARC may be a spin-on-glass (SOG) such as DUO™ that is manufactured by Honeywell Corporation. In other processes where the Low-k dielectric layer is a Low-k polymer material, the base material of the sacrificial ARC material may be a spin-on-polymer (SOP) that has a polymeric backbone similar to that of the SiCOH dielectric layer. For example, the polymeric backbone of the SOP may be poly(norbornene), polystyrene, poly(p-phenylene), polyxylene, polyimide, and polyarylene.

In order to make the ARC layer non-reflective, chemists include additives that reduce or eliminate reflectivity. These additives are included in the sacrificial ARC base material, and may be a reflective material that shifts the phase of the outgoing light to cancel the incoming light; a refractive material, a reflective and refractive material, a refractive and absorbent material, or any combination of these additives. These additives are generally proprietary.

Following the photoresist patterning step, the trench in Step 3 (refer to Figure 1) is etched into the SiCOH dielectric layer to form the structure illustrated in Step 3. The etching process is applied for a time sufficient to form a trench having the desired depth. The etch chemistry chosen to etch the trench should remove the sacrificial ARC material, sometimes referred to as a Sacrificial Light Absorbing Material, or SLAM, at a slightly faster rate than it removes the SiCOH dielectric layer, to avoid formation of defects. The trench may be etched using the same equipment and etch chemistry that had been used previously to etch the via in Step 1 (refer to Figure 1).

Ask The Experts

Q: In the fab, is it possible to dry etch (plasma or reaction ion etch) tantalum?

A: There is some newer work on using reactive ion etching to remove thin films of tantalum using tetrachlorosilane:argon (SiCl4:Ar) plasmas. Researchers at the University of Edinburgh studied the etching characteristics with respect to the SiCl4:Ar ratio, plasma power and chamber pressure. They found that increasing the flow rate of SiCl4 or plasma power leads to an increase in the etching rate. However, they observed that increasing the flow rate of Ar to more than 30 sccm (standard cubic centimeters per minute) and/or the plasma pressure to more than 100 mTorr did not provide any additional benefit.

Course Spotlight: SILICON PHOTONICS TECHNOLOGY AND APPLICATIONS

OVERVIEW

The proliferation of cloud computing and artificial intelligence is driving significant performance improvements in data center processing. Unfortunately, the connections between these servers, and even the connections between the boards in these servers, is limiting performance and driving up power dissipation. Silicon photonics promises a solution to these problems. Compared to standard integrated circuit technology, silicon photonics technology requires fundamentally different thinking about fabrication, packaging, testing, reliability and failure analysis. This course delves into the fabrication, packaging, testing, reliability and analysis of these circuits. ***Silicon Photonics Technology and Applications*** is a 2-day course that details the vital technologies required to understand optics and photonics; photonics integrated circuits; silicon photonics and its packaging and systems; and future applications and materials.

This skill-building series is divided into six segments:

1. **Photonics Integrated Circuits (PIC).** Participants will learn the fundamentals of photonics, and how these signals are generated and detected on a chip. They will also learn about the techniques to split optical signals, combine optical signals, and merge optical signals for long distance communications.

2. **Electronic Integrated Circuits (EIC).** Participants will learn the fundamentals of the electronic circuits associated with silicon photonics. They will also learn about the circuits that work to convert the optical signals back and forth into electrical data, and waveforms that can be used by other data processing chips.

3. **Silicon Photonics Packaging.** Participants will learn about 2-dimensional and 3-dimensional approaches to packaging that can enable enhanced performance; smaller form factors; and improved bandwidth densities. This includes heterogeneous integration elements like Through-Silicon Vias (TSVs), copper pillars, and high-performance substrates.

4. **Technology Roadmaps.** Participants will learn how this industry is evolving through better component integration. This includes developments in laser technology, packaging technology, and sensing technology. This course will cover the IEEE Heterogenous Integration Roadmap, and its sections on Integrated Photonics, as well as Defense Electronics roadmapping activities.

5. **On-Board Optics (OBO), Near-Package Optics (NPO), and Co-Packaged Optics (CPO).** Participants will learn about the history of OBO and the development of "pluggable optics"; how OBO brings silicon and optics together in a package to reduce power and latency; about NPO, where the optical circuitry is placed on the printed circuit board close to the electrical circuitry; and CPO, which provides superior performance and lower thermal dissipation.

6. **Systems and Applications.** Participants will learn about the developing applications and systems that will use silicon photonics.

COURSE OBJECTIVES

1. This course will help participants understand the foundational concepts of silicon photonics, and identify the advantages of integrating photonics with electronics.

2. The participants will learn about the manufacturing processes for photonic integrated circuits (PICs).

3. The participants will explore hybrid and heterogeneous integration techniques, analyze the design principles of passive photonic components, and understand the role of waveguides in optical communication.

4. This course will evaluate the functionality of active devices in silicon photonics systems; discuss the role of silicon photonics in optical interconnects and communication systems; and explore the breadth of applications enabled by silicon photonics.

5. The participants will assess the impact of silicon photonics on various industries, understand the workflow from design to fabrication, and identify key challenges facing silicon photonics technology.

6. This course will identify future trends and opportunities in this rapidly evolving field.

COURSE OUTLINE

DAY 1

1. What is Silicon Photonics?
   a. Introduction
   b. The Electromagnetic Spectrum and the C, L, and O Bands for communication

2. Photonic Integrated Circuits (PIC)
   a. Fabrication
   b. Passive Devices
   c. Active Devices
   d. Integration
   e. Interconnects
   f. A Comparison of Passive and Active Devices

3. Packaging Roadmap and Industry Trends
   a. IEEE Heterogeneous Integration Roadmap
   b. Examples of Photonics Applications and Trends from the Industry
      1. Luxtera
      2. Ayar Labs
      3. Intel
   c. Fiber Optics Effects
   d. Optical Link Budgets
   e. Industry Trends
   f. Electronics
      1. Power Dissipation
      2. Thermal Dissipation

4. Co-Packaged Optics and DARPA PIPES
   a. Co-Packaged Optics
   b. DARPA PIPES Program

DAY 2

5. Pluggables, Near-Package Optics, and CPO
   a. Pluggable Products
   b. On-Board Optics
   c. Near-Package Optics
   d. Co-Packaged Optics
   e. Performance Evolution and the Need for CPO
   f. Example Silicon Photonics Packaging

6. Fiber Optic Cables
   a. Basics
   b. Single Mode Fiber (SMF) Cables
   c. Multi-Mode Fiber (MMF) Cables

7. Silicon Photonics Applications
   a. Defense Electronics
   b. Autonomous Vehicle Wiring
   c. Data Center/Artificial Intelligence
   d. Future PIC Materials

8. Course Wrap-up Discussions and Q&A
   a. Silicon Photonics Market Information
   b. Summary
   c. References
   d. Websites

Upcoming Courses:

Public Course Schedule:

Silicon Photonics Technology and Applications - July 16-17, 2025 (Wed.-Thurs.) | San Jose, CA - $1,195 until Wed. Jun. 25

Failure and Yield Analysis - September 29-October 2, 2025 (Mon.-Thurs.) | Phoenix, AZ - $2,095 until Mon. Sept. 8

Wafer Fab Processing - November 3-6, 2025 (Mon.-Thurs.) | Phoenix, AZ - $2,095 until Mon. Oct. 13

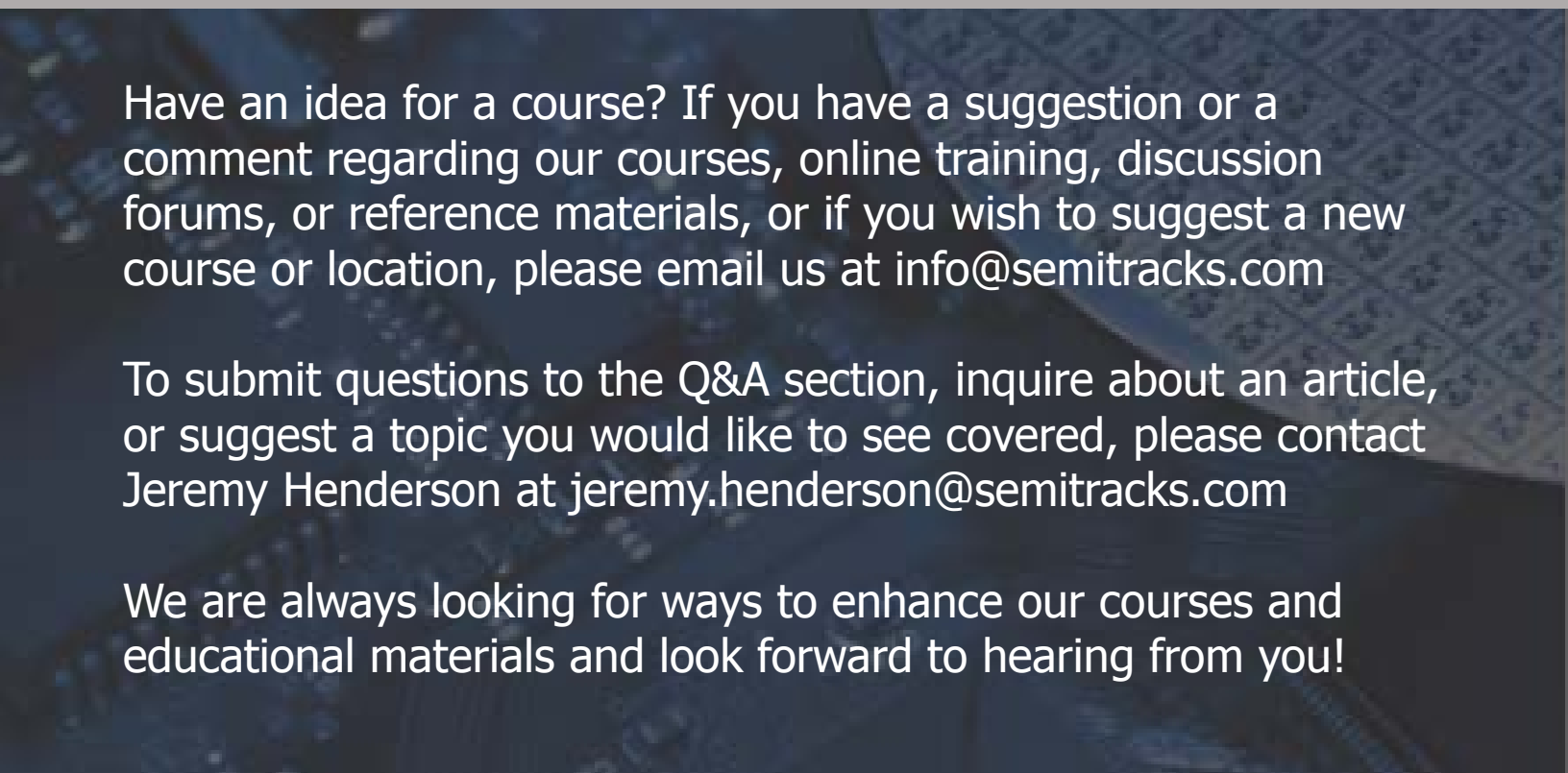
Defect-Based Testing - February 19-20, 2026 (Thurs.-Fri.) | Munich, Germany - $1,195 until Thurs. Jan. 29

Wafer Fab Processing - February 23-26, 2026 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Feb. 2

Failure and Yield Analysis - March 2-5, 2026 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Feb. 9

Semiconductor Reliability and Product Qualification - March 9-12, 2026 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Feb. 16

EOS, ESD and How to Differentiate - March 16-17, 2026 (Mon.-Tues.) | Munich, Germany - $1,195 until Mon. Feb. 23



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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!