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YOUR QUARTERLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Transfer Molding

By Christopher Henderson

In this quarter's Feature Article, we continue our series on Transfer Molding. Transfer Molding is one of the more common steps in semiconductor packaging, and provides protection for the sensitive semiconductor components and packaging interconnect. We will continue our discussion of transfer molding by focusing on additional characterization tests used to assess mold compounds.

The next test we will briefly discuss is epoxy resin mold compound breakdown voltage (BV) testing. One concern is the degradation of the breakdown voltage in epoxy resin mold compounds over time when the material is exposed to high temperatures for extended periods of time, referred to as a High Temperature Operating Life Test, or HTOL test, shown in the two graphs on the next page. Figure 1 shows the raw data, and the ratio of the HTOL breakdown voltage versus the breakdown voltage at time zero. We highlight the control devices, that received no HTOL stress at the top in gold, the other units that received post cure in green, and the units that did not receive the additional post cure, just the standard 175°C, 4-hour cure, in blue. Notice that there is also one outlier, shown in red.

WHAT'S INSIDE?

Want to take control of your learning? See page 6

Upcoming Courses:

- IC Packaging Technology
- Advanced CMOS/FinFET Fabrication
- Reliability and Product Qualification
- Wafer Fab Processing
- Failure and Yield Analysis

See page 10 for more details

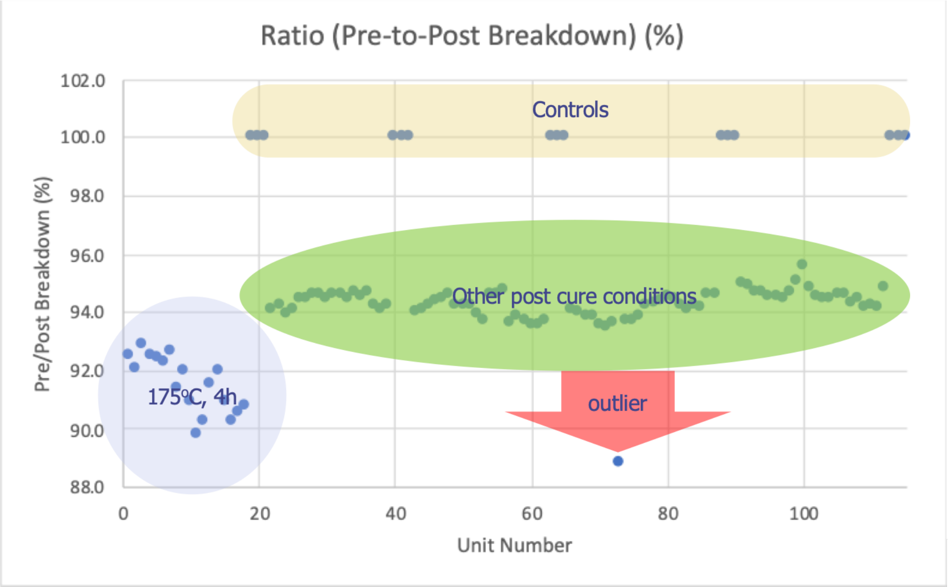


Figure 1- Data showing breakdown voltages before and after HTOL testing.

Let's look at the information in a little more detail. Figure 2 shows the data from Figure 1 as a delta-breakdown voltage degradation after a stress test of 125°C and 6 hours, along with a number of control units that were not exposed to high temperature. The first group, labeled in green on the graph, underwent a standard post cure of 175°C and 4 hours, while the remaining components underwent post cures at longer times and/or higher temperatures, shown in red on the graph. While the first group shows significant degradation after the standard cure conditions of 175ºC and 4 hours, the other time and temperature combinations generally show only a 40 to 50% degradation in the breakdown voltages. We see that a post cure makes a definite improvement of breakdown voltages.

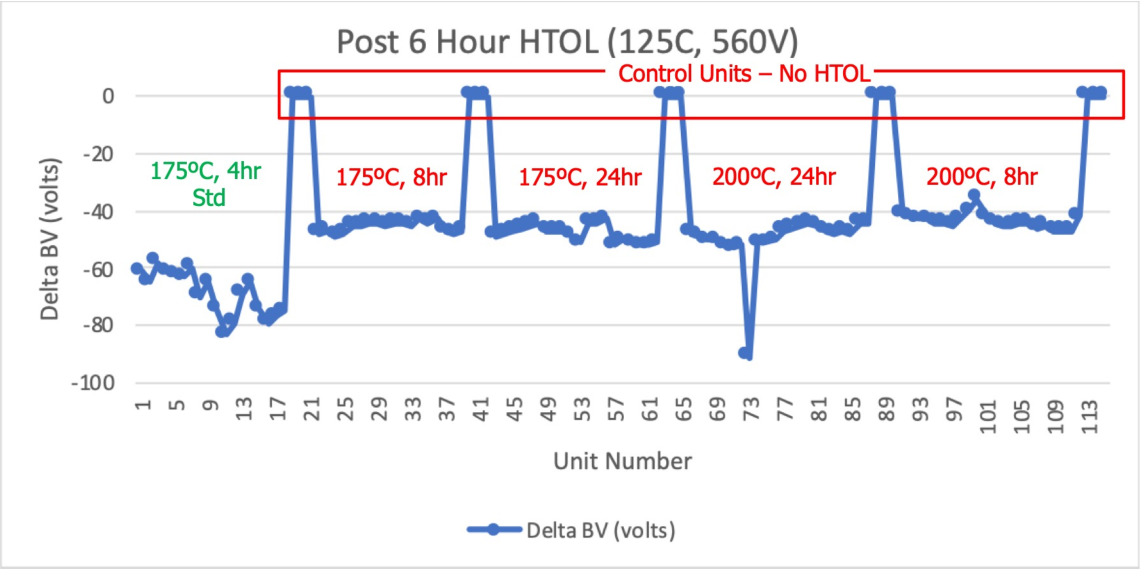


Figure 2- Breakdown voltage shown as a difference (or delta) plot before and after HTOL stress testing.

Electrical performance of the epoxy resin mold compound depends on the compatibility of the material with the semiconductor die. One way to envision this is to think about the epoxy resin mold compound in conjunction with the passivation overcoat layer. For the epoxy resin mold compound, one must also account for the differences in electrical characteristics between the resin and the filler particles. The electromagnetic equations (shown below) for understanding electrical performance are basic, but the shape and geometry of the package, and the filler particles play an important role.

$$E = \frac{V}{d}$$

$$D = \varepsilon_0 \varepsilon^* E \text{ and } \Delta D = Q$$

We show a cross-section view of the package in Figure 3 for reference. For charge, one would need to calculate the charge at the interface between the components. This will change the electrical properties of the components and content.

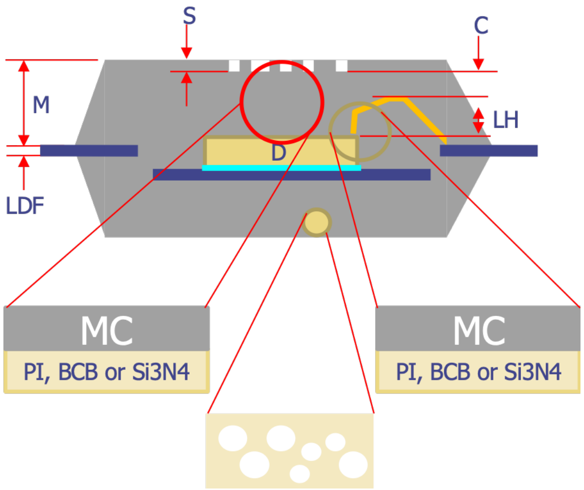


Figure 3- Cross-sectional view of a typical mold-encapsulated product.

Engineers will calculate the dielectric properties from measurements, and also use them for charge estimation. It is important to understand that this is not something that is studied by epoxy resin mold compound suppliers, so manufacturers are not likely to have data available at low frequencies to provide to you to help you estimate charge. There is also no data for passivation, since it is highly dependent on the deposition process. With that said, the passivation layer properties can be estimated using these two equations,

$$\varepsilon_r = 3.2 + \chi^*(\omega)$$

$$\sigma_0 = 10^{-15} \text{ S/m}$$

where the dielectric constant ε_r is modeled by χ^*, which is a function of the frequency; and conductivity (σ_0), which is measured in Siemens per meter. These are sometimes used as default values. From this, we can estimate the interface charge, and then determine the dielectric permittivity of different phases of the epoxy resin mold compound curing process.

In Figure 4, we show some example data on the Sumitomo epoxy resin mold compound we have been using as an example. The angular frequency ranges from µHz to MHz, which corresponds to a time scale ranging from 1µsec to 277 hours.

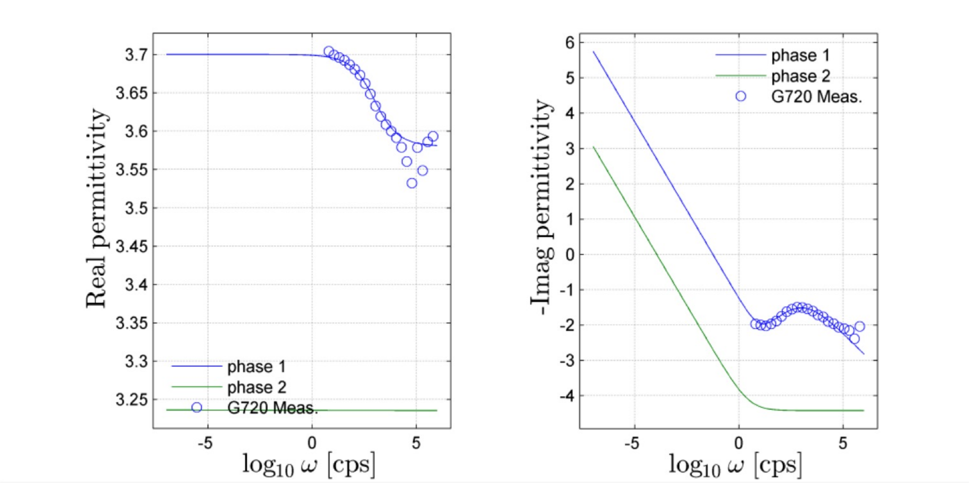


Figure 4- Sumitomo mold compound permittivity as a function of frequency (cycles per second – cps).

Next, we can estimate the charge in the epoxy resin mold compound. Figure 5 shows this estimation. A discontinuity in the electrical displacement field creates interfacial charge, and this charge is frequency dependent. This is also known as interfacial polarization. A similar polarization would be observed in epoxy resin mold compound since it is a composite material with dielectric properties.

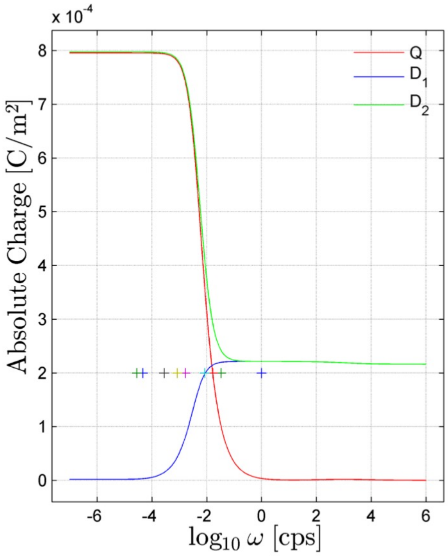


Figure 5- Absolute charge as a function of frequency for the Sumitomo mold compound.

In next quarter's Feature Article, we will continue our discussion of transfer molding by continue our discussion of the electrical properties of mold compounds and additional characterization tests used to assess mold compounds.

Technical Tidbit – Silicon Carbide's Advantages in Power Electronics

In this month's Technical Tidbit, we will discuss Silicon Carbide's advantages in Power Electronics. Silicon Carbide (SiC) has rapidly emerged as a dominant force in power electronics, leaving traditional silicon (Si) in the dust for high-performance applications. Its intrinsic material properties make it an absolute powerhouse for efficient energy conversion.

Here is why SiC is considered the ideal material for next-generation power electronics:

- The first advantage is ultra-low power losses and high voltage blocking. Due to the scaling relationship between specific on-resistance and breakdown voltage ($R_{ON} \sim V_B^{2.5}$), SiC can handle immensely high blocking voltages while keeping conduction losses remarkably low compared to traditional Si, as shown in Figure 1.
- The second advantage is high-temperature operation. SiC devices can operate reliably at extreme temperatures—even up to 225°C—without creating significant leakage. This robustness dramatically simplifies thermal management, paving the way for compact electronic systems with simplified cooling units.
- The third advantage is fast switching with minimal loss. SiC unipolar devices enable exceptionally fast switching speeds. Furthermore, SiC Schottky barrier diodes exhibit zero reverse recovery, which slashes dynamic power losses and significantly optimizes power efficiency.
- The fourth advantage is excellent native oxide formation. A major manufacturing perk is that SiC allows for wide-range doping and thermal oxidation to naturally form a silicon dioxide (SiO2) insulating layer. This unique trait makes the fabrication of reliable, commercial MOS devices like power MOSFETs highly effective.

These important advantages drive major real-world benefits, including a 20–36% energy saving in heavy train drives, an 80% power module volume reduction, and a notable 5% fuel efficiency improvement in modern electric vehicles like the Tesla Model 3.

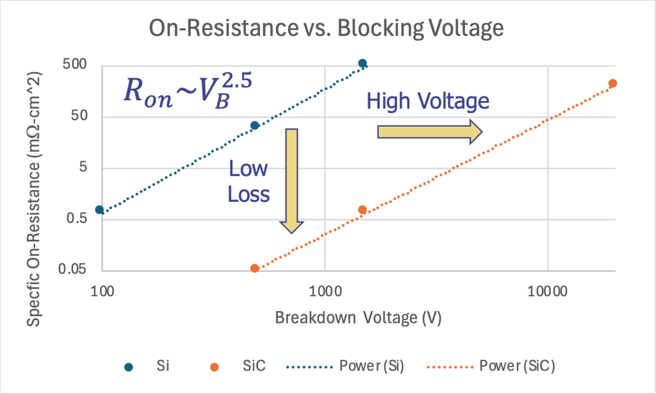
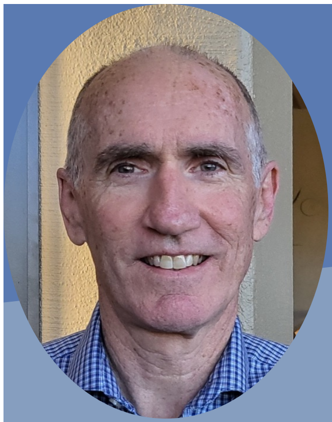


Figure 1- Specific On Resistance (R_{ON}) as a function of blocking voltage for both SiC and Si.

In conclusion, SiC delivers significantly improved power efficiency, and enables compact electronic systems with simplified cooling.



Ask The Experts

Q: Can you explain more about how accurate heat assessment of heat distribution is possible in glass substrates?

A: Thermal imaging in conjunction with glass substrates can be very powerful. This allows for a more accurate assessment of heat distribution across a device due to their uniform thermal behavior. This can be crucial for thermal management strategies, facilitating better heat sink designs, and contributing to the overall reliability of electronic components. Companies like InfraTec GmbH make IR cameras that can perform this work. These systems can be equipped with spectral filters in a filter wheel. Filters will be individually adjusted according to the specific glass of the customers. On the one hand, these filters allow measuring the surface temperature of glass without any impact on the transmission radiation of objects behind glass. On the other hand, measurements of objects with high temperature behind glass can be carried out without having an influence on the glass surface temperature. For more details about this, contact InfraTec directly.

Course Spotlight: IC PACKAGING TECHNOLOGY

OVERVIEW

Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: 1) pitch conversion between the fine features of the IC die and the system level interconnection; 2) chemical, environmental and mechanical protection; 3) heat transfer; 4) power, ground and signal distribution between the die and system; 5) handling robustness; and 6) die identification among many others. Numerous critical technologies have been developed to serve these functions; technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

IC Packaging Technology is a 2-day course that details the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available; how technologies interact; what choices must be made for a high-performance product vs. a consumer device; and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing; processes; and materials selection, tailoring, and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

By focusing on current issues in packaging technology, participants will learn why advances in the industry are occurring along certain lines and not others. Participants will learn about semiconductor packaging without having to delve heavily into the complex physics and materials science that normally accompany this discipline. Participants will learn basic, but powerful aspects about the semiconductor packaging. This skill-building series is divided into four segments:

1. **Molded Package Technologies.** Participants will learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.

2. **Flip Chip Technologies.** Participants will learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.

3. **Wafer Level Packages.** Participants will learn the newest technologies that enable the increasingly popular Wafer Chip Scale Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).

4. **Through Silicon Via Packages and Future Directions.** Participants will understand the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

COURSE OBJECTIVES

1. The course will supply participants with an in-depth understanding of package technologies, current and future.
2. Potential defects associated with each package technology will be highlighted to enable the participants to identify and eliminate such issues in product from both internal assembly and OSAT houses.
3. Cu and solder plating technologies will be described with special emphasis on package applications in Through Silicon Vias (TSVs) and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void-free thermal aging performance, and contamination-free interfaces.
4. New package processes employed in TSV production will be described, along with current cost reduction thrusts, to enable the participants to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. This course will provide detailed references for participants to study and further deepen their understanding.

COURSE OUTLINE

DAY 1

1. The Package Development Process as a Package Technology
   - a. Materials and Process Co-Design

2. Molded Package Technologies
   - a. Die Attach
     - i. Plasma Cleans
   - b. Wire Bonding
     - i. Au vs. Cu vs. Ag
     - ii. Die Design for Wire Bonding
   - c. Lead Frames
   - d. Transfer and Liquid Molding
     - i. Flash
     - ii. Incomplete Fill
     - iii. Wire Sweep
     - iv. Green Materials
   - e. Pre- vs. Post-Mold Plating
   - f. Trim and Form
   - g. Saw Singulation
   - h. High Temperature and High Voltage Materials

DAY 2

1. Flip Chip and Ball Grid Array Technologies
   - a. Wafer Bumping Processing
     - i. Cu and Solder Plating
     - ii. Cu Pillar Processing
   - b. Die Design for Wafer Bumping
   - c. Flip Chip Joining
   - d. Underfills
   - e. Substrate Technologies
     - i. Surface Finish Trade-Offs
     - ii. Core, Build-up, and Coreless
   - f. Thermal Interface Materials (TIMs) and Lids
   - g. Fine Pitch Warpage Reduction
   - h. Stacked Die and Stacked Packages
     - i. Material Selection for Board Level Temperature Cycling and Drop Reliability

2. Wafer Chip Scale Packages
   - a. Redistribution Layer Processing
   - b. Packing and Handling
   - c. Underfill vs. No-Underfill

3. Fan-Out Wafer Level Packages
   - a. Chip First vs. Chip Last Technologies
   - b. Redistribution Layer Processing
   - c. Through Mold Vias

4. Through Silicon Via Technologies
   - a. Current Examples
   - b. Fundamental TSV Process Steps
     - i. TSV Etching
     - ii. Cu Deep Via Plating
     - iii. Temporary Carrier Attach
     - iv. Wafer Thinning
   - c. Die Stacking and Reflow
   - d. Underfills
   - e. Interposer Technologies: Silicon, Glass, Organic

5. Surface Mount Technologies
   - a. PCB Types
   - b. Solder Pastes
   - c. Solder Stencils
   - d. Solder Reflow

Upcoming Courses:

IC Packaging Technology – September 14-15, 2026 (Mon.-Tues.) | Phoenix, AZ – $1195.00 until Mon. Aug. 24

Advanced CMOS/FinFET Fabrication – September 21-22, 2026 (Mon.-Tues.) | Phoenix, AZ – $1195.00 until Mon. Aug. 31

Semiconductor Reliability and Product Qualification – February 1-4, 2027 (Mon.-Thurs.) | Cambridge, UK – $2,095 until Mon. Jan. 18

Advanced CMOS/FinFET Fabrication – February 16-17, 2027 (Tues.-Wed.) | Dresden, Germany – $1195.00 until Tues. Jan. 26

Wafer Fab Processing - February 22-25, 2027 (Mon.-Thurs.) | Dresden, Germany – $2,095 until Mon. Feb. 1

IC Packaging Technology – March 3-4, 2027 (Wed.-Thurs.) | Munich, Germany – $1195.00 until Wed. Feb. 10

Failure and Yield Analysis - March 8-11, 2027 (Mon.-Thurs.) | Munich, Germany – $2,095 until Mon. Feb. 15

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!