

InfoTracks

Semitracks Monthly Newsletter

Thin Film Photovoltaics Technology

Solar power-- the clean, renewable energy source of the future-- is becoming more and more crucial to our economic and environmental welfare.

Read more, Page 3



Future Memory Technologies – Part 3

By Christopher Henderson

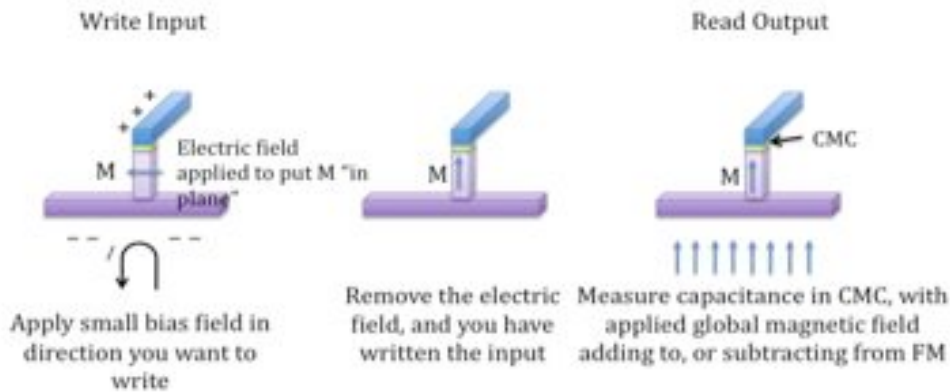


Figure 1. Basic concept behind magnetic nanopillar memory operation.

Researchers are also investigating other types of memories for the future. As we approach the limitations imposed by physics on charge-based memories, new architectures will be needed to scale down further. One potential memory technology that is generating some interest is magnetic nanopillars. Another commonly used acronym for nanopillar technology is RAMA. It stands for reconfigurable array of magnetic automata. Researchers have already demonstrated that a random array of up and down polarized ferromagnetic pillars

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SEMITRACKS, INC.

Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

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(CoFe₂O₄) embedded in a ferroelectric or multiferroic matrix (e.g., BiFeO₃) can have their magnetizations rotated from being perpendicular to the pillar (and the film) surface to being in-the-plane of the film with the application of a modest electric field.

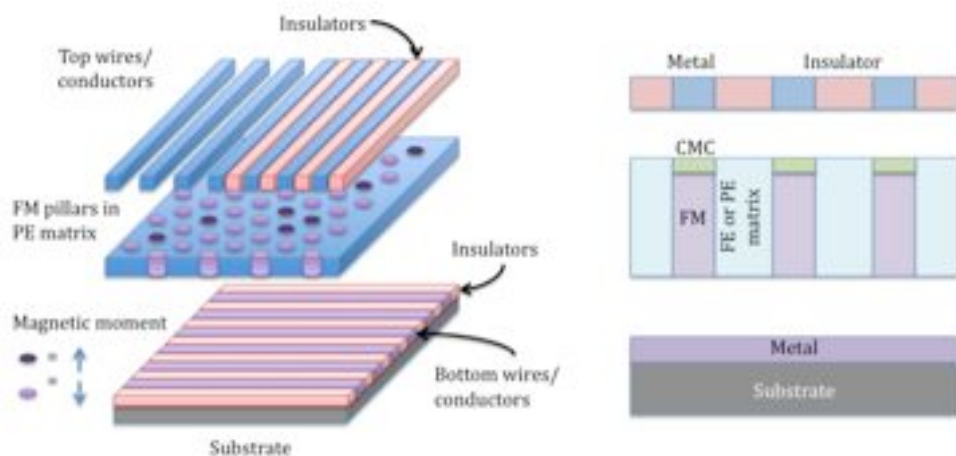


Figure 2. Construction of magnetic nanopillar devices.

This technique is being explored to create magnetic nanopillar devices. Wires are formed on a substrate using nanoimprint lithography, electron beam lithography, or other lithographic techniques. The ferromagnetic pillars are constructed through lithographic methods or polymeric self-assembly. The

ferroelectric material resides in columns within the piezoelectric material or matrix to form potential connections between two conducting planes. The lower part of the ferromagnetic material forms the nanopillar, while the top portion is the colossal magnetocapacitive material, such as LaPrCaMnO₃, LaSrMnO₃ or other manganite. This material is called a colossal magnetocapacitive (CMC) material, because such a capacitor built of this compound can exhibit large changes in capacitance with changes in magnetic field. Patterning metal, etching the material where it is not needed, and depositing insulating material between the conductors form the top connections. Researchers at the University of Virginia and others have described this type of approach.

Table 1. Comparison of Magnetic Nanopillar or RAMA with standard CMOS SRAM technology.

Device	CMOS ca. 2020	RAMA
Operation Method	Ballistic Charge	Magnetic exchange (dipolar)
Fabrication method	Photolithography	Polymeric self-assembly
Cost	High	Low
Cell size	100nm	20nm
Bit density	10 ¹⁰ cm ⁻³	~ 10 ¹³ cm ⁻³
Switching energy	5aJ/op	0.01aJ/op
Speed	0.1 ps	< 1ns
Non-volatility (No stand-by power)	No	Yes
RT operating	Yes	Yes
CMOS compatibility	---	Yes

Notice that RAMA, or nanopillar technology has some potentially significant advantages over standard memory technology. Notice that the nanopillar technology can be made through polymeric self-assembly, potentially reducing the cost of the device. The cell size can be smaller, allowing for greater bit density. The switching energies are much lower than for standard memory, but the switching speeds are also much lower. RAMA can also be made to be compatible with existing CMOS processing.

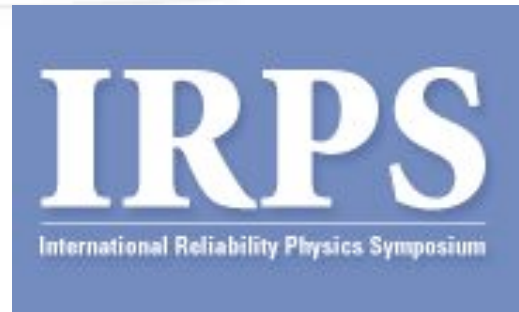
Ask the Experts

Q: What types of techniques can be used to highlight bond pad cratering?



A: One technique that can highlight bond pads for cratering using an optical microscope is nickel decoration. The aluminum bondpad is etched away, and the chip is placed in a nickel plating solution for several minutes. The nickel will first adhere to the cracks, providing contrast in the optical microscope.

*To post, read, or answer a question, [visit our forums](#).
We look forward to hearing from you!*



**April 10-14, 2011
Monterey, CA, USA**

For nearly 50 years, IRPS has been the premier conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic assemblies through an improved understanding of both the physics of failure as well as the application environment.

If you would be interested to meet with Semitracks personnel at IRPS, please call or e-mail us.

*Learn more about this conference at:
<http://www.irps.org/>*



Thin Film Photovoltaics Technology Spotlight

There are actually two major technology groups working on solar energy: silicon crystalline technology, and thin film technology. Since the 1980s, stunning breakthroughs in thin-film photovoltaic technology have made clean, light-generated electricity more feasible and economical. Many people believe that thin-film technologies might ultimately be the most cost-effective method to bring solar energy to the world on a large scale. As many companies rapidly introduce new technologies to harness solar power, tracking developments--let alone understanding them--can be daunting. Semitracks' one-day Thin Film Photovoltaics Technology course analyzes and distills the most important aspects of this complex technology.

Learn more at:

<http://www.semitracks.com/index.php/en/courses/public-courses/photovoltaics/thin-film-photovoltaics-technology>

Online Training Photovoltaics Material

If you are interested in the area of Photovoltaics, but aren't able to attend the upcoming courses; we encourage you to explore the option of our Online Training system.

Our online semiconductor training courses can be customized for your job function. The structure of the material allows you, the user, to learn when you have a few moments free, alleviating the need to carve a large block out of your schedule. Other disciplines allow you to cross-train for potential promotions or transfers or to simply do a better job in your current position. The material is always current and interactive, allowing you to learn the material easily. You can search our databases for answers to questions you might have or simply use it as a reference.

If you aren't quite ready to sign up for an account, please contact us at info@semitracks.com and we will create a temporary two-week account for you to try out our system.



Upcoming Courses

[EOS, ESD and How to Differentiate](#)

April 4-5, 2011 – Penang, Malaysia

[Wafer Fab Processing](#)

April 25-28, 2011 – Kuala Lumpur, Malaysia

[IC Packaging Metallurgy](#)

May 9-10, 2011 – Munich, Germany

[Failure and Yield Analysis](#)

May 10-13, 2011 – Munich, Germany

[Semiconductor Reliability](#)

May 16-18, 2011 - Munich, Germany

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or e-mail us at info@semitracks.com.

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by email at jeremy.henderson@semitracks.com.

We are always looking for ways to enhance our courses and educational materials.

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