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Semitracks Monthly Newsletter

Wire-Wound Resistors

By Christopher Henderson

This month, we will continue our series of Feature Articles by discussing the Wire-Wound Resistor.

Wire-wound resistors consist of a metal wire or ribbon wrapped around a cylinder. The cylinder can be made from either plastic or ceramic. The wire ends would be welded to metal end caps. The structure would then be either conformally coated or encapsulated with some type of mold injection material, similar to a plastic packaged integrated circuit.

Figure 1 shows an exterior view of a wire-wound resistor. One can see the end caps on the right and left of the cylindrical structure which houses the resistor element or elements.

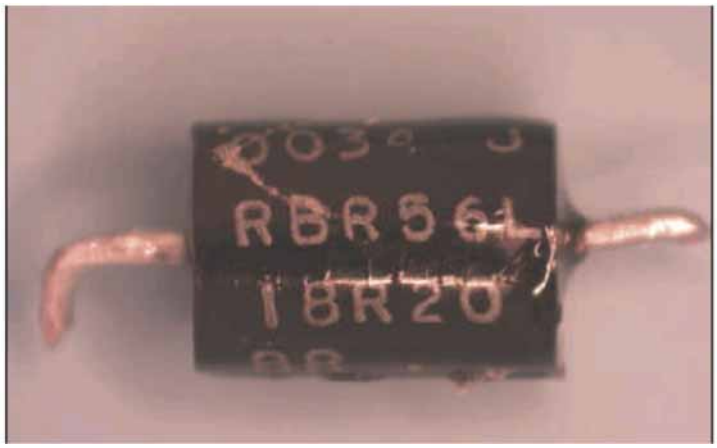

Figure 1. Exterior view of a wire-wound resistor.

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Figure 2 shows an x-ray radiograph of the resistor. One can see the two wound sections of the resistor between x and y, and between y and z.

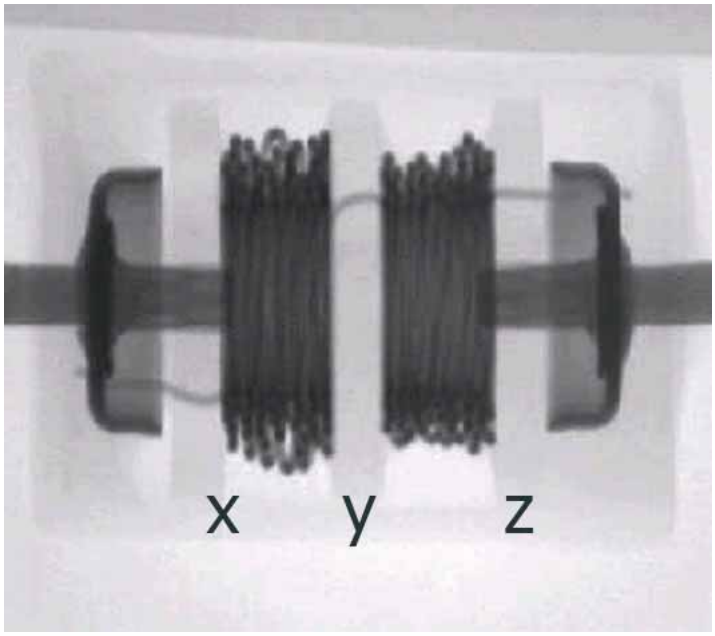


Figure 2. X-ray view of the resistor showing the wound sections.

Let's discuss some typical failure mechanisms one might encounter with wire-wound resistors. First is electrical overstress. This is typically in the form of a fused wire within the elements. Second is separation of the resistance wire element from the termination. This can result from inadequate wire stress relief with differences in the thermal coefficients of expansion, which leads to mechanical stress and overload. Third is corrosion of the resistance wire or terminal. While corrosion of wire-wound resistors is not as prevalent as corrosion with hybrid chip resistors, they still must be protected from moisture if the electronic system operates in a moisture-rich environment. Fourth is mechanical damage to the resistance wire. This would normally be something caused by the supplier. We should note that some suppliers actually use mechanical grinding to trim lower value resistors to the correct value.

In next month's Feature Article, we will conclude the topic of resistors by discussing several case histories.

Technical Tidbit

Qualification By Similarity (QBS)

In this month's Technical Tidbit, we will cover qualification by similarity.

Let's begin by explaining why Qualification By Similarity, or QBS, is important. QBS allows the product engineer to qualify a product with a reduced set of tests, so this can save a considerable amount of time and effort associated with the qualification process, and lower the cost to the manufacturer. However, this can only occur under certain conditions. The die in the product to be qualified needs to share common technology and fabrication process with other dice. The package for the product to be qualified needs to share a common format, fabrication and assembly process with other products that use this package. And most importantly, the product we plan to qualify needs to share these characteristics with a product that has already successfully passed a full qualification. These shared characteristics constitute a qualification family, so let's discuss a qualification family in more detail. The qualification standards we use discuss these principles.

JEDEC JESD47 contains a high-level statement concerning qualification families. It states that while JESD47 may be used to qualify an individual component, it is designed to also qualify a family of similar components utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs. Interactive effects of the silicon and package per JEP156A must be considered in applying family designations.

AEC-Q100 defines qualification families. A qualification family first and foremost shares a common wafer fab technology, whether it be CMOS, NMOS, BiCMOS, or bipolar. Second, within the wafer fab process, it should also have the following important elements in common: technology feature size, substrate material and doping, the same number of masks and lithographic process, the same doping process, gate structure, polysilicon, oxidation process, interlayer dielectrics, metallization, passivation, and die backside preparation. Also, a qualification family must share the same wafer fab site.

At the assembly level, the qualification family should also share a number of common characteristics. It should use the same overall assembly process, whether it be ceramic or plastic. It should also share the same package type with the same cross-sectional dimensions, die paddle dimensions, and substrate base material. The individual elements of the assembly process should also be the same, like the leadframe base material and plating, the die attach material, the wire bond material, size and process, the plastic mold compound material, the solder ball metallization system, and the heat sink dimension and materials. Finally, the assembly site must be the same for the qualification family.

Both JEDEC JESD47 and AEC-Q100 describe a process for qualifying multiple sites. If one plans to qualify the process at multiple sites, one should use one or more lots from each site. The qualification test vehicles should be one lot of a device that is sensitive to the changed attribute, and 3 lots total from the most sensitive families. The high-level steps include: identifying all of the products affected by the process change, identifying the critical structures affected by the change, identifying the potential failure modes and mechanisms, defining the groups and providing justification, providing the qualification test plan, and demonstrating process capability at each step for each of the affect process steps.

Ask the Experts

Q: What is the polymer layer comprised of in a Multilayer Metal Tape?

A: The companies that manufacture this tape may consider the polymer layer to be a trade secret, so they may not list it in their product catalogs. However, there are some likely options. The polymer can be Polyimide, Benzocyclobutene (BCB), Bismalemide Triazine (BT), or some other high glass-transition temperature polymer.

Spotlight: Advanced CMOS/FinFET Fabrication

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" Advanced CMOS/ FinFET Fabrication is a 1-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

WHAT WILL I LEARN BY TAKING THIS CLASS

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs and FD-SOI are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including ion implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.
2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.
3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.
4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

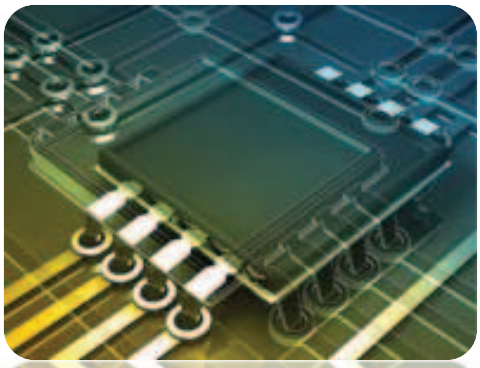
1. The seminar will provide participants with an in-depth understanding of SOI technology and the technical issues.
2. Participants will understand how Hi-K/Metal Gate devices are manufactured.
3. Participants will also understand how FinFET devices are manufactured.

4. The seminar provides a look into the latest challenges with copper metallization and Low-k dielectrics.
5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.
6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.
7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.
8. Finally, the participants see a comparison between FD-SOI (the leading alternative) and FinFETs.

COURSE OUTLINE

1. Advanced CMOS Fabrication – Introduction
2. Front End Of Line (FEOL) Processing
    a. SOI and FD-SOI
    b. Ion Implantation and Rapid Thermal Annealing
    c. Pulsed Plasma Doping
    d. Hi-K/Metal Gates
    e. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
3. Back End Of Line (BEOL) Processing
    a. Introduction and Performance Issues
    b. Copper
        i. Deposition Methods
        ii. Liners
        iii. Capping Materials
        iv. Damascene Processing Steps
    c. Lo-k Dielectrics
        i. Materials
        ii. Processing Methods
    d. Reliability Issues
4. FinFET Manufacturing Overview
    a. Substrates
        i. Bulk
        ii. SOI
    b. FinFET Types
    c. Process Sequence
    d. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology

5. FinFET Reliability
   a. Defect density issues
   b. Gate Stack
   c. Transistor Reliability (BTI and Hot Carriers)
   d. Heat dissipation issues
   e. Failure analysis challenges
6. Future Directions for FinFETs
   a. Comparison of FD-SOI and FinFETs – Are FinFETs a better choice?
   b. Scaling



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Webinars

(Click on each item for details)

Wafer Fab Processing

4 sessions of 4 hours each
Europe: April 6 – 9, 2021 (Tue – Fri),
1:00 P.M. – 5:00 P.M. CET
US: April 19 – 22 (Mon – Thur),
9:00 A.M. – 1:00 P.M. PST

IC Packaging Technology

4 sessions of 4 hours each
Europe: April 19 – 22, 2021 (Mon – Thur),
1:00 P.M. – 5:00 P.M. CET
US: April 12 – 15, 2021 (Mon – Thur),
9:00 A.M. – 1:00 P.M. PST

Advanced CMOS/FinFET Fabrication

4 sessions of 2 hours each
Europe: April 26 – 29, 2021 (Mon – Thur),
3:00 P.M. – 5:00 P.M. CET
US: April 5 – 8, 2021 (Mon – Thur),
9:00 A.M. – 11:00 A.M. PST