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YOUR QUARTERLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Transfer Molding

By Christopher Henderson

In this quarter's Feature Article, we continue our series on Transfer Molding. Transfer Molding is one of the more common steps in semiconductor packaging, and provides protection for the sensitive semiconductor components and packaging interconnect. We will continue our discussion of transfer molding by focusing on the test used to characterize mold compound materials and packages that use mold compound materials.

First, let's look at Differential Scanning Calorimetry, or DSC. In Figure 1, we show DSC data for a Sumitomo epoxy resin mold compound formulation as an example. This method of display shows normalized curves setting the initial heat capacity as the reference. The first run, or first heating is shown in blue. During this run, the epoxy resin mold compound will cure. The second run, or second heating, is shown in red. In this run, the epoxy resin mold compound is already cured. The Sumitomo G720 compound is a multi-aromatic ring and multifunctional high voltage mold compound. In the first run, three cure peaks are visible, labeled 1, 2, and 3, in the graph. Since 2 and 3 are very close to each other with regards to delta Q, with only a small dip in between, 2 and 3 may be indistinguishable, so only 2 peaks may be observable.

WHAT'S INSIDE?

Want to take control of your learning? See page 8

Upcoming Courses:

- Failure and Yield Analysis
- Reliability and Product Qualification
- IC Packaging Technology
- Advanced CMOS/FinFET Fabrication
- Wafer Fab Processing

See page 12 for more details

The low temperature peak at 120°C is related to the transfer mold processing. The high temperature peak at 260°C is for performance improvements. Changes in the dielectric properties will also indicate the curing characteristics.

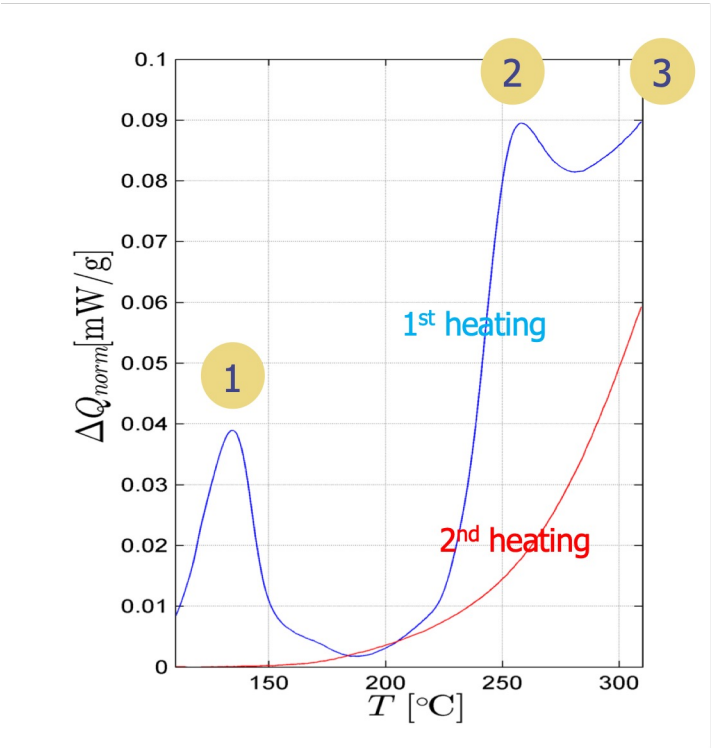

Figure 1- Differential Scanning Calorimetry (DSC) data for a Sumitomo epoxy resin mold compound formulation.

Let's address some questions associated with DSC. First, let's make a comment about the graphs in Figure 2, since they are somewhat different than the graph in Figure 1. These graphs show DSC curves comparing the of amount of energy input, shown on the Y-axis, required to maintain each temperature, shown on the X-axis, across a range of temperatures. The first question is what do we mean by residual cure? Is it the remainder of the process associated with peak 1, or a continuation of the process associated with peaks 2 and 3, as shown in the graph on the left? This is something that would require input from the epoxy resin mold compound developer as to what is happening. The second question is why are there different processes, or reacting components, in the mold compound? They assist in epoxy resin mold compound cure solidification, and provide better adhesion to the leadframe, but do they affect operation on the semiconductor die? The third question pertains to the solder reflow process. Does the solder reflow at 260°C affect the epoxy resin mold compound properties? We see these peaks at approximately 260°C in both graphs. During the second heating, the DSC curves deviate from the zero reaction lines, which are shown as the black lines in the graphs. This would indicate that something is occurring. Again, these are questions for the epoxy resin mold compound supplier.

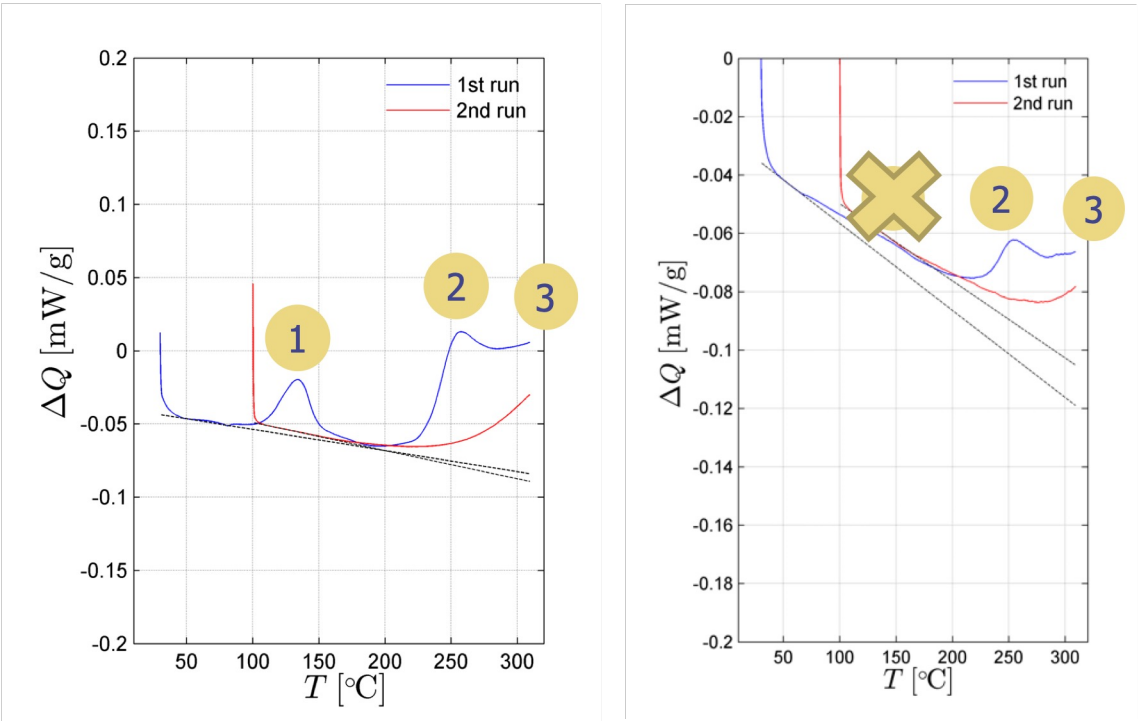

Figure 2- DSC curves comparing the of amount of energy input required to maintain each temperature, across a range of temperatures.

In Figure 3, we show a graph from the Sumitomo epoxy resin mold compound on the left, and a different epoxy resin mold compound on the right - a Shin-Etsu epoxy resin mold compound formulation. We use the same procedure for each formulation. Notice that the two samples show clear differences. There is very little thermal activity in the Shin-Etsu epoxy resin mold compound in the first heating region.

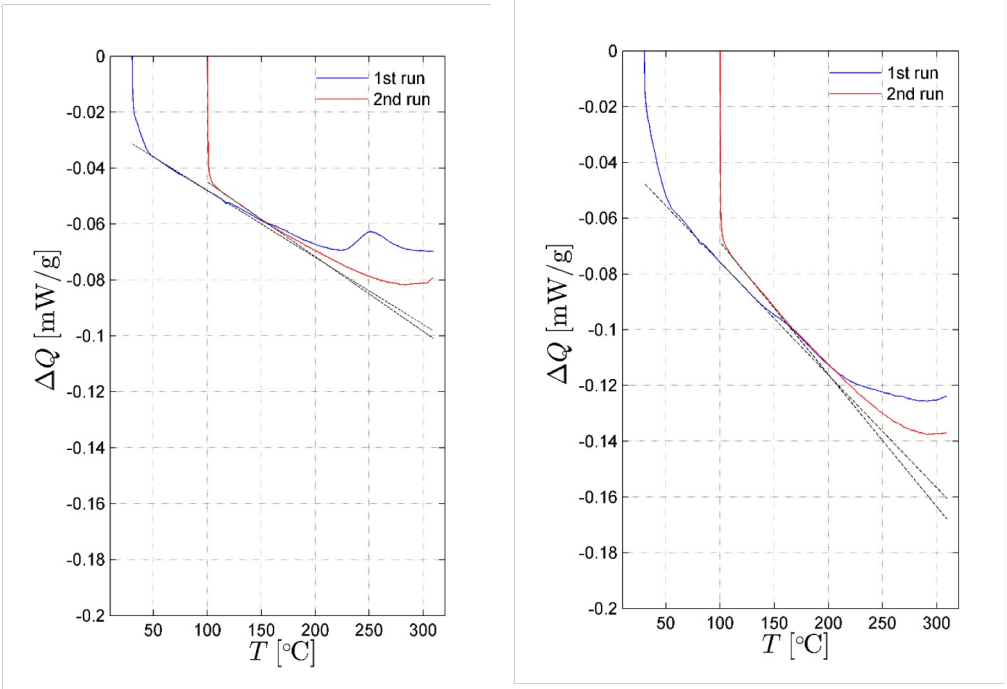

Figure 3- DSC Curves for two epoxy resin mold compounds: the Sumitomo compound previously discussed (left), and a Shin-Etsu compound (right).

Let's move on and briefly discuss a characterization test for epoxy resin mold compound shear strength, known as the button shear test. In Figure 4, we show testing on several epoxy resin mold compound formulations, labeled Sample 1 through Sample 6, in conjunction with different substrates. In general, the higher modulus materials do not easily mold into packages. Furthermore, a lower modulus tends to yield better adhesion. This button shear test is not completely accurate, but does provide a relative metric for adhesion. Since we mold packages through compression, a shear test provides somewhat different data.

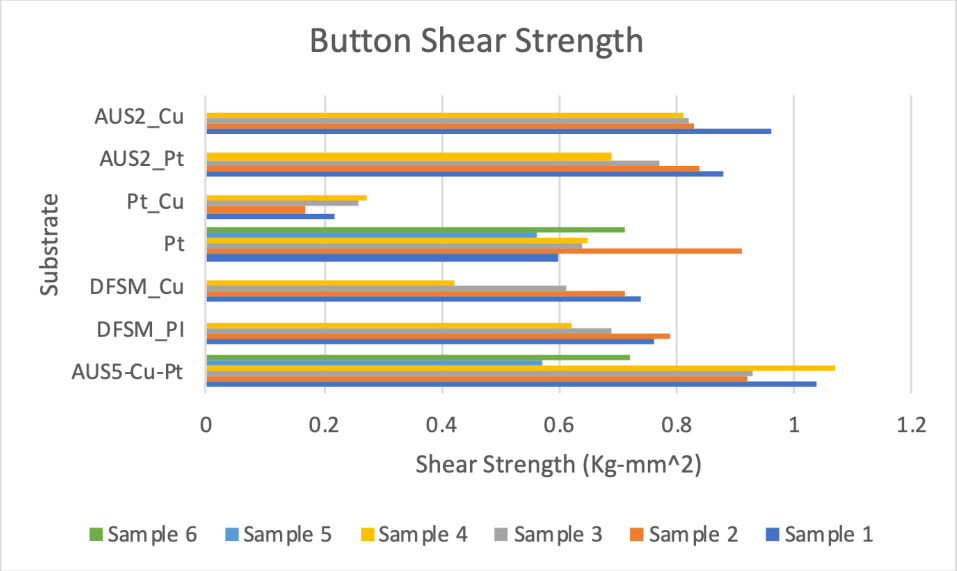

Figure 4- Mold compound shear strength in rank order of modulus (highest on top and lowest on bottom).

In next quarter's Feature Article, we will continue our discussion of transfer molding by covering additional characterization tests used to assess mold compounds.

Technical Tidbit – Contact Field Plates

In this month's Technical Tidbit, we will discuss the Contact Field Plate (CFP). Contact Field Plates can be used to improve the reliability of Laterally Diffused Metal Oxide Semiconductor (LDMOS) transistors, in particular by reducing Hot Carrier Injection (HCI).

Before we discuss the Contact Field Plate, let's first review some concepts regarding the LDMOS transistor. We show an example cross-section diagram of an LDMOS transistor in Figure 1. The LDMOS transistor is a type of transistor with an extended drain region. This Drain-Extension, as shown in Figure 1, is designed to create lower electric fields in the drain region, allowing the transistor to operate at higher voltages than a normal n-channel MOSFET in a given technology. This extension increases the drain-to-channel depletion region when the transistor is in the off-state, or in saturation. Since carriers "drift" in the electric field associated with the drain-to-channel depletion region, this region is often referred to as a "drift region" in an LDMOS transistor.

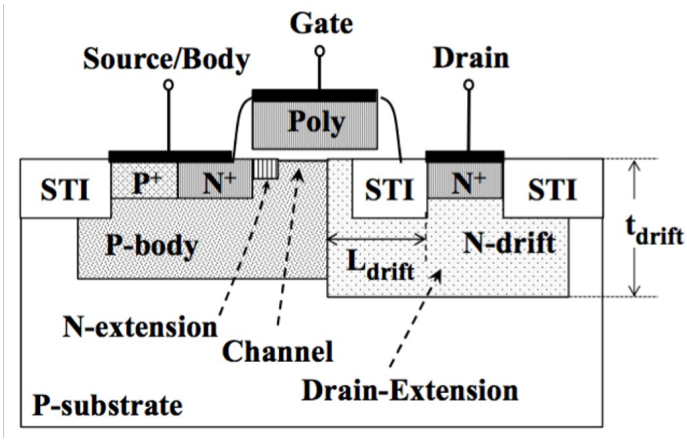

Figure 1- Example cross-section diagram of an LDMOS transistor (after El-Kareh).

One method for extending the length of the drift region is to use Shallow Trench Isolation to create a longer length for the drift region. The use of Shallow Trench Isolation (STI) allows device engineers to create a more compact transistor structure by creating both lateral and vertical drift regions to extend the overall drift region. The drawback to using STI to increase the length of the drift region is that it can also increase $R_{DS}(on)$, so let's briefly discuss $R_{DS}(on)$. $R_{DS}(on)$ is a critical circuit parameter for power transistors. To understand the components of $R_{DS}(on)$, refer to Figure 2. Here is the equation for $R_{DS}(on)$.

$$R_{DS}(on) = R_S + R_D + R_{ch} + R_{drift} + R_{acc}(\Omega)$$

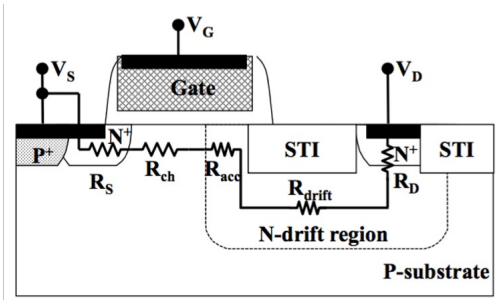

Figure 2- Cross-section diagram showing the components of $R_{DS}(on)$ in an LDMOS transistor.

There are several components that need to be controlled and minimized. They include the source series resistance, the drain series resistance, the resistance in the main drift region, the resistance in the drain region that is affected by surface accumulation, when the gate is positive with respect to the drift region, and the channel resistance, which is modulated by the gate voltage. $R_{DS}(on)$ is also a function of the device area, which is the product of the device pitch and the device width.

Since the STI region increases $R_{DS}(on)$, is there another method for increasing the drift region without this negative side-effect? One solution is to use a Contact Field Plate (CFP). The CFP can be biased to help push the carriers deeper into the silicon. The CFP is typically made with tungsten, since tungsten can make contact with the silicon without any adverse effects. The CFP can also help create a Reduced Surface Field, sometimes known as RESURF. For further details on RESURF, we recommend our Online Training Course on Process Integration. The cross-section simulation images in Figure 3 help to show the movement of carriers deeper in the silicon. The tungsten CFP is visible in the three images on the right as the rectangular region just to the right of the gate (shows up as blue in the top- and middle-right images, and as gray in the bottom-right image.

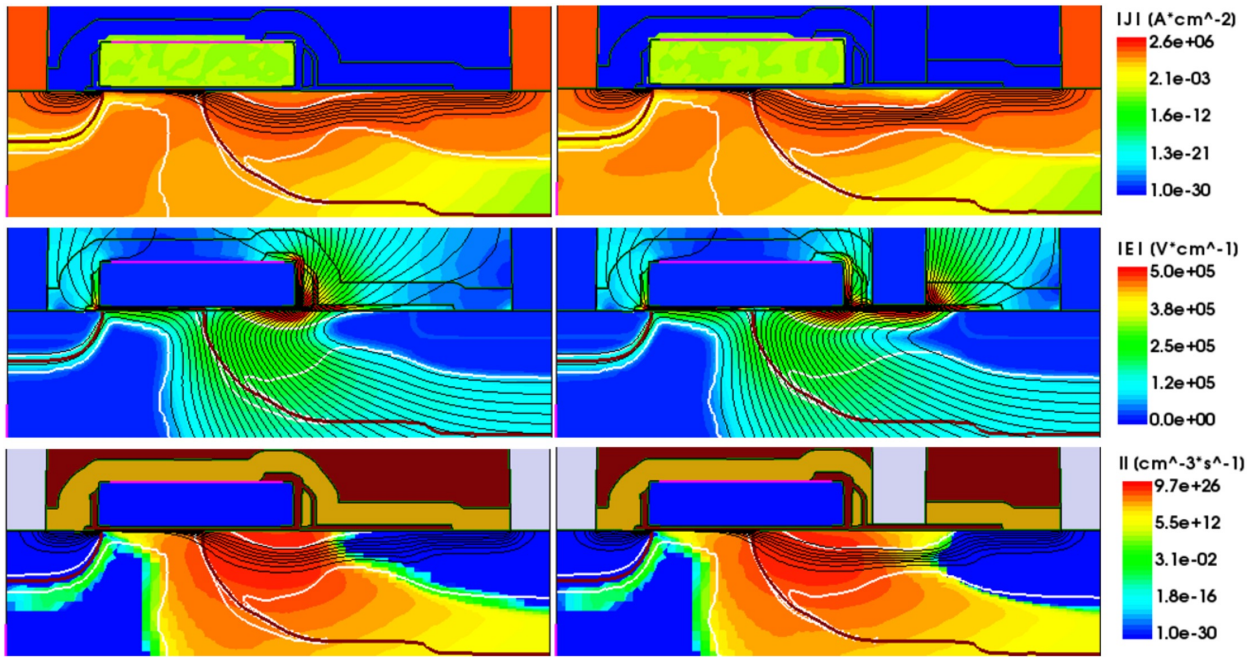

Figure 3- On-state simulations at V_{DS} ≈12V and V_{GS} =2V for the default FA device (left) and default CFP device (right). Top: Magnitude of current density (|J|) and current potential lines (black lines). Middle: Magnitude of electric field (|E|) and potential lines (black lines). Bottom: Impact ionization (II) and current potential lines (black lines). The CFP depletes the underlying silicon which bends the current route more into the bulk. Moreover, this results in two more moderate field peaks instead of the strong field peak at the gate edge, thereby reducing the impact ionization and hence increasing BV_{ON}. (J. Toonen, Master's Thesis, , p.53, 2019, Eindhoven University of Technology)

In conclusion, the CFP can be used to reduce $R_{DS}(on)$ while creating an increased drift region. While the technique may not lead to compact LDMOS transistor structure, it can help reduce both the resistance and the size of the transistor.

Ask The Experts

Q: Does the F in BF_2 cause etching during ion implant?

A: Yes, the Fluorine (F) in BF_2 ion implantation can cause etching-like effects, particularly in the form of surface roughing and chemical reactions that create gaseous products. While not a traditional "liquid or plasma wet etch" process, the presence of F in the silicon lattice, particularly during high-dose implants and subsequent annealing, leads to chemical interactions that cause surface damage and can result in unwanted material removal or degradation. A good reference for this particular issue would be C. J. Viera, et.al., "BF_2^+ implant: a fluorine bubble induced ET failure," ASMC 2002.

Course Spotlight: SEMICONDUCTOR RELIABILITY AND PRODUCT QUALIFICATION

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms, and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability; assessing the impact of new materials; dealing with limited margins, and other factors. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. ***Semiconductor Reliability and Product Qualification*** is a 4-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants will learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product. This skill building series is divided into four segments:

1. **Overview of Reliability and Statistics.** Participants will learn the fundamentals of statistics, sample sizes, distributions and their parameters.

2. **Failure Mechanisms.** Participants will learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, and others.

3. **Qualification Principles.** Participants will learn how test structures can be designed to help test for a particular failure mechanism.

4. **Test Strategies.** Participants will learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The course will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.

2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.

3. The course will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.

4. The course will offer a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.

7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

DAY 1

1. Introduction to Reliability
   a. Basic Concepts
   b. Definitions
   c. Historical Information

2. Statistics and Distributions
   a. Basic Statistics
   b. Distributions (Normal, Lognormal, Exponent, Weibull)
   c. Which Distribution Should I Use?
   d. Acceleration
   e. Number of Failures

DAY 2

3. Overview of Die-Level Failure Mechanisms
   a. Time Dependent Dielectric Breakdown
   b. Hot Carrier Damage
   c. Bias Temperature Instability
   d. Electromigration
   e. Stress Induced Voiding
   f. BEOL Dielectric Reliability

4. Package Level Mechanisms
   a. Moisture/Corrosion
      i. Failure Mechanisms
      ii. Models for Humidity
      iii. Tja Considerations
      iv. Static and Periodic stresses
      v. Exercises
   b. Thermo-Mechanical Stress
      i. Models
      ii. Failure Mechanisms
   c. Chip-Package Interactions
      i. Low-k fracture
   d. Through Silicon Via Reliability
   e. Thermal Degradation/Oxidation

DAY 3

5. Board Level
   a. Package Attach (Solder) Reliability
      i. Creep/Sheer/Strain
      ii. Lead-Free Issues
      iii. Electromigration/Thermomigration
      iv. MSL Testing
   b. Board Level Reliability Mechanisms
      i. Interposer
      ii. Substrate

6. Use Condition Failure Mechanisms
   a. Electrical Overstress/ESD
   b. Radiation Effects

7. Test Structures and Test Equipment

8. Developing Screens, Stress Tests, and Life Tests
   a. Burn-In
   b. Life Testing
   c. HAST
   d. JEDEC-based Tests

DAY 4

9. Calculating Chip and System Level Reliability

10. Developing a Qualification Program
    a. Process
    b. Standards-Based Qualification
    c. Knowledge-Based Qualification
    d. MIL-STD Qualification
    e. JEDEC Documents (JESD47H, JESD94, JEP148)
    f. AEC-Q100 Qualification

11. JEDEC Tests

12. Exercises and Discussion

Upcoming Courses:

Failure and Yield Analysis - April 13-16, 2026 (Mon.-Thurs.) | San Jose, CA - $2,195

Semiconductor Reliability and Product Qualification - April 20-23, 2026 (Mon.-Thurs.) | San Jose, CA - $2,095 until Mon. Mar. 30

IC Packaging Technology – September 14-15, 2026 (Mon.-Tues.) | Phoenix, AZ - $1195.00 until Mon. Aug. 24

Advanced CMOS/FinFET Fabrication – September 21-22, 2026 (Mon.-Tues.) | Phoenix, AZ – $1195.00 until Mon. Aug. 31

Advanced CMOS/FinFET Fabrication – February 16-17, 2027 (Tues.-Wed.) | Dresden, Germany – $1195.00 until Tues. Jan. 26

Wafer Fab Processing - February 22-25, 2027 (Mon.-Thurs.) | Dresden, Germany - $2,095 until Mon. Feb. 1

IC Packaging Technology – March 3-4, 2027 (Wed.-Thurs.) | Munich, Germany - $1195.00 until Wed. Feb. 10

Failure and Yield Analysis - March 8-11, 2027 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Feb. 15

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!