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Soft ESD Failures

[Part 2, By Chris Henderson]

this issue:

The second part of this series covers soft ESD failure mechanisms in plastic packages. In this article, we cover three case histories where charging was found to be a problem in plastic-packaged components. The first occurred in 1988 at Signetics during solder reflow in Japan. The second occurred at Delco, the electronics subsidiary of General Motors, in 1993. This work was the first to be published at a public conference. In fact, this group of failures led to the generation of an Automotive Electronics Council specification to diagnose and mitigate the problem. The third failure occurred in 1999 in ICs mounted next to high voltage television tubes.

One of the earliest reports of plastic package failures due to charging, or soft ESD, was at Signetics assembly operations in Japan. Their factories reported plastic-packaged components failing after board reflow assembly. Some components recovered when removed from the printed circuit boards while others did not. These components exhibited high supply current and some leakage on certain I/O pins. The components did not recover with a short, low temperature bake (70 degrees centigrade for 12 hours) but did recover with a higher temperature bake (150 degrees centigrade for 16 hours). All failed components that were decapsulated recovered immediately upon decapsulation. These components also recovered when exposed to x-ray radiation at 110 kV accelerating voltage for 12 minutes. The problem was eventually fixed by installing charge neutralization on the reflow furnaces.

The engineers at Signetics traced the problem to air flow across the surface of the plastic packages that resulted in triboelectric charging. Air flow in the ovens caused the top of the IC package to be charged to a negative voltage around -5kV. During the reflow operation, the epoxy becomes somewhat conductive, allowing charge to work through the package to the die glassivation layer and charge that layer negative. When the component cools after the reflow operation, the charge is trapped on the surface of the passivation as the epoxy returns to a more electrically insulating state. The charge on the passivation affects the transistors and parasitic structures on the IC, creating leakage on the supplies and at the I/O pins.

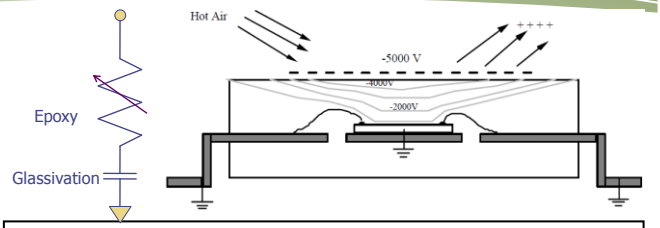


Figure 1: Diagram showing charge build-up on an integrated circuit package.

The charge inverts the n-epitaxial region, causing p-implanted resistors to become leaky to the p-isolation regions. The charging also changes the resistor values and transistor characteristics. Specifically, in the transistors, it led to changes in the low current beta values. The charging also created increased junction leakage and lower junction breakdown voltages.

Figure 1 illustrates the behavior of the plastic and the glassivation layer. The top of the package is charged triboelectrically. The glassivation layer forms a capacitor. The epoxy thermoset forms a variable resistor; as the temperature increases, the resistivity of the epoxy decreases, allowing the capacitor to charge. When the epoxy cools, it becomes an insulating material and traps the charge on the glassivation layer, which is still acting like a capacitor. The active structures on the die are then affected by the charge on the top of the glassivation layer. Engineers at NXP refined this model and presented their work at the 2008 International Reliability Physics Symposium. For more information, see M. van Soestbergen, et. al., "Electrical Characterization of Plastic Encapsulation Using an Alternative Gate Leakage Method," Proc. IRPS, 2008, pp. 462-467.

Even the purest of epoxies exhibits a low level of ionic contamination. As the epoxies are heated, the ionic contaminants begin to move about more easily, lowering the effective resistance of the material. On the following page, Table 1 shows the effective resistance of five types

TABLE 1 Epoxy Bulk Resistivity in Ω-Cm vs temp

Temp (°C)	EME1100HS	EME6210S	EME6210SR	EME1100HJ	Nitto HC10-2
50	1.50E+16	4.00E+15	4.20E+15	8.00E+15	1.50E+16
75	7.40E+15	1.40E+15	2.50E+15	4.50E+15	1.00E+16
100	1.80E+15	5.00E+14	8.50E+14	1.10E+15	1.50E+15
125	3.50E+14	1.30E+14	2.40E+14	3.30E+14	2.00E+14
150	9.50E+13	3.30E+13	4.20E+13	9.70E+13	7.00E+13
175	8.00E+12	9.80E+11	1.20E+12	8.10E+12	3.00E+12
200	4.00E+10	2.70E+10	3.30E+10	3.50E+10	1.50E+11

TABLE 2 Time in seconds to charge die to 100 volts

50	4.92E+04	1.31E+04	1.38E+04	2.63E+04	4.92E+04
75	2.43E+04	4.60E+03	8.21E+03	1.48E+04	3.28E+04
100	5.91E+03	1.64E+03	2.79E+03	3.61E+03	4.92E+03
125	1.15E+03	4.27E+02	7.88E+02	1.08E+03	6.57E+02
150	3.12E+02	1.08E+02	1.38E+02	3.18E+02	2.30E+02
175	2.63E+01	3.22E+00	3.94E+00	2.66E+01	9.85E+00
200	1.31E-01	8.86E-02	1.08E-01	1.15E-01	4.92E-01

Note: Die area .25 x .25 cm Passivation 2μ , Electro static charge 5KV, Epoxy 0.095 cm thick

of epoxies at seven different temperatures ranging from 50 degrees to 200 degrees centigrade. Table 2 shows the times required to charge the die surface to 100 volts for the same epoxies and the same seven temperatures. At high temperatures, the die surface can charge in less than one second.

Figure 2 shows the epoxy resistances plotted in terms of resistance as a function of temperature. As the epoxies heat through the glass transition temperature, the resistance begins to drop more markedly.

Figure 3 shows the time to charge data as a function of temperature. The time to charge drops dramatically as the temperature increases. For this experiment, the engineers at Signetics used the following parameters: a 0.25 x 0.25 cm die in the package, a .095cm-thick plastic over the die, a lid voltage of 5000 volts, a 2-micron-thick passivation, and a 1-dimensional model with no lateral bleed.

In the 1980s, when several electronics subsidiaries of major automotive manufacturers encountered a soft ESD failure mechanism, they devised a test to rate components for gate leakage sensitivity that was included in the AEC Q100-006 specification. The test places a needle probe source with a high voltage on the lid of the package. The components sit on a grounded plate in an oven and are heated to a specified temperature. The voltage is applied to the lid, the components are cooled to room temperature, and, finally, they are measured for leakage. The test normally applies 400 volts to the lid. Figure 4 shows the probe needle inside the oven (left) and a close up view of the needle (right) with respect to the component.

Engineers and scientists at NXP proposed an alternative method for measuring gate leakage at IRPS in 2008. They determined that better gate leakage results occur if the post mold cure temperature is increased. Raising the temperature from 175°C to 190°C appears to tie up mobile ions in the mold compound more effectively. However, higher temperatures can lead to increased bondwire intermetallic formation. Many researchers question the merit of changing the process since these failures tend to be marginal instances of minor leakage. No field failures have been observed. Furthermore, affected ICs would get better in the field. Finally, the test methods to identify this mechanism have problems, such as slow throughput and long test times.

A number of issues occur with the proposed test method. The specification calls for setting the voltage on the lid to -400 volts, but there is no way to precisely measure the voltage since the probe influences the measurement. The proposed system for grading gate leakage on the components is not consistent. The times and temperatures for the charging conditions are arbitrary. There is no turnkey test system available. Furthermore, not much data chronicles how manufacturing problems related to components passing or not passing the gate leakage test. Finally, there is no practical solution other than adding another metal layer

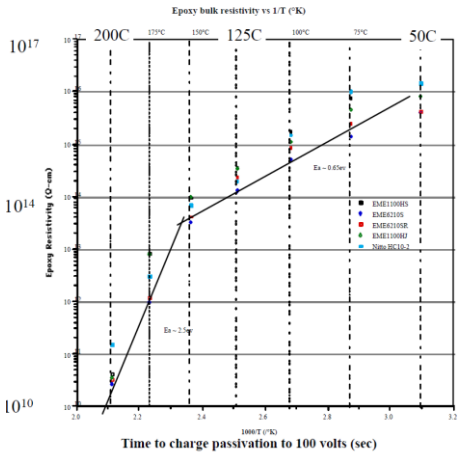
Figure 2 (top right): Epoxy resistances plotted as a function of temperature. The resistance decreases rapidly, especially above the glass transition temperature. Figure 3 (bottom right): The corresponding time to charge decreases rapidly as the temperature increases.

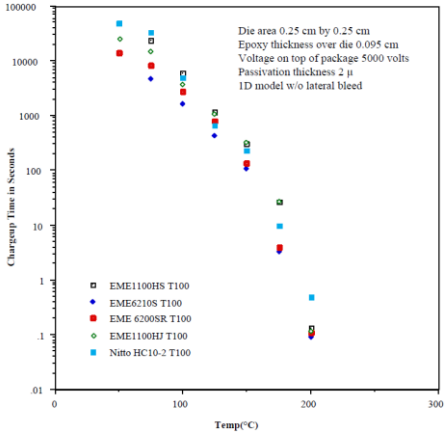
to the IC or package for field plating. This step would increase component costs substantially.

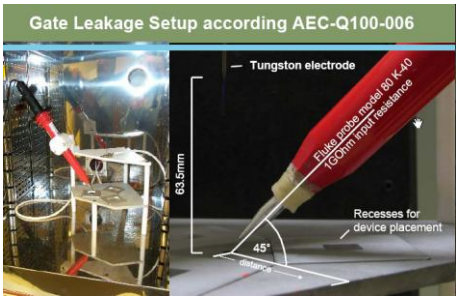
The diagram on the following page shows some of the problems associated with the voltage measurement. A Fluke high voltage probe is used to measure the potential at a certain height over the component. However, one typically encounters a steep voltage drop when moving away from the center position under the electrode. This is different than one would expect based on field lines.

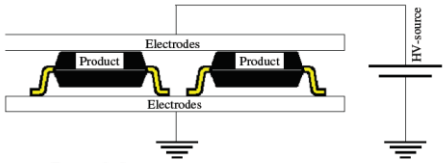
Another potential problem with the gate leakage specification is the

Figs. 4-6 show a proposed Automotive Electronics Council standard for testing charge buildup within an integrated circuit package.









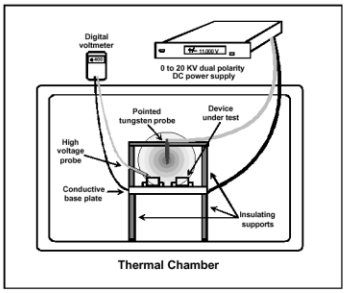


Figure 1: GL test fixture and set-up

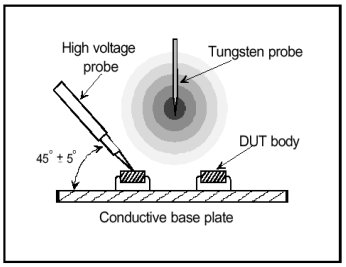
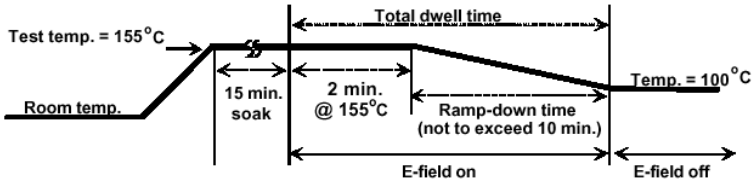


Figure 2: Measurement angle used to monitor E-field voltage

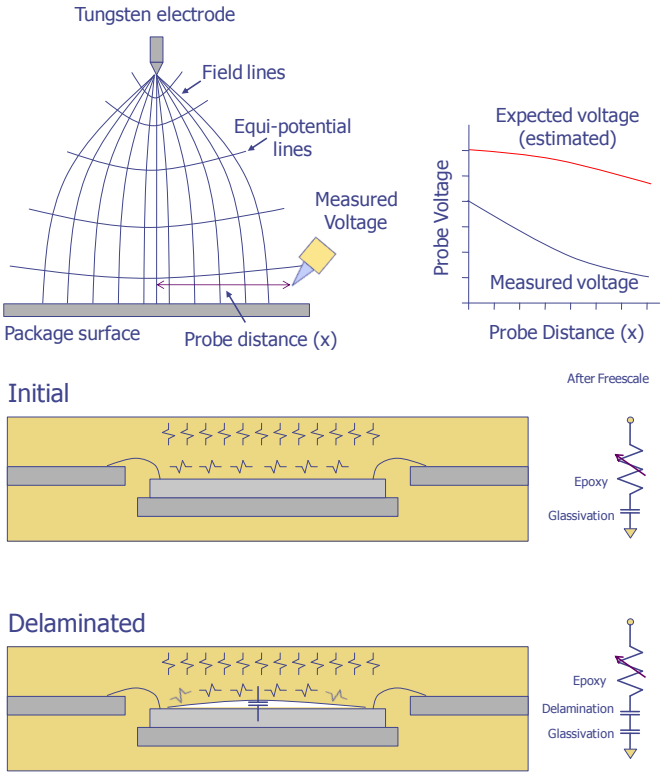


presence of a delamination between the package and die, or lack thereof. The delamination adds another capacitive element into the circuit, fundamentally altering the voltage that couples to the IC glassivation layer.

The third case history associated with the soft ESD mechanism in plastic packages is a Philips Semiconductor high voltage analog component. Engineers at Philips discovered this device was failing during biased temperature testing. The components exhibited bipolar base channel leakage and collector-emitter leakage. As a result, a parametric shift or functional failure occurred in the analog section. The problem worsens if the high voltage bond pad is near a sensitive analog circuit node. The charge can also spread through the plastic during burn-in or operation. Like the gate leakage problem just discussed, sensitive transistors can be found using a high voltage probe as a stimulus. Engineers have done limited studies on this mechanism, but the indications are that this mechanism is strongly accelerated by temperature. The activation energy is approximately 2.5 electron-volts, which is similar to hydrogen-based ionic movement. The problem can be mitigated by using field plating on the die layout or by using a die coat.

The trend in the semiconductor industry is toward thinner packages and larger die. In a thin package, it is easier to charge the die glassivation due to lower resistance path through the plastic to the die. With a larger die, the center of the die is farther from the bond wires that could bleed off some charge, so therefore it is more likely to store charge. Another important trend is toward lead-free components. A lead free process is hotter, so the epoxy is more conductive and quicker to pick up charge. However, it is also quicker to lose it when cooling down, unless popcorn delaminations have occurred. More metal layers improve shielding from the charge and new processes have higher doping and are less surface sensitive.

Here is a summary of soft ESD failures. The electrical symptoms include I/O leakage due to increased transistor channel currents, abnormal characteristics on unrelated circuit blocks, and higher than normal supply currents. The circumstantial symptoms include multiple failures at



Figs. 6-9: Current-voltage (I-V) curves (top), silicon-silicon dioxide band diagram for basic EPROM structure (bottom), and triboelectric charging potential for various materials (right).

electrical test after packaging, or board assembly, components that initially pass, then fail a subsequent test, and components with thin glassivation or packaged in thinner packages. Some other failure mode characteristics include recovery after x-ray radiography, recovery after decapsulation, and the ability to duplicate the failure mode with a static gun after decapsulation.

Some areas of uncertainty and further research include the conduction process in epoxy and the choice between low and high conduction plastics, lead free processes, popcorn delamination, and triboelectric charging during board assembly, including sources and effective remedies.

Announcements

SEMICON West

July 13-15 • San Francisco, CA

The SEMICON West 2010 show will present a full program of exhibitions, presentations, meetings, and workshops focused on 3D interconnects (3D IC) for integrated circuits. Show exhibitors in the 3D IC segment, including Applied Materials, Tokyo Electron, Lam Research, and SÜSS MicroTec, represent the industry's largest gathering of 3D IC leading companies at one event. Semitracks will be offering three courses during the event: Photovoltaics Overview, Photovoltaics Technology and Manufacturing, and Reliability Challenges.

Upcoming Courses

Wafer Fab Processing

June 14-17 • Enschede, Netherlands

Photovoltaics Overview

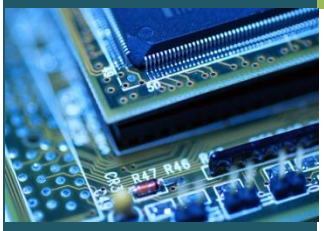
July 12 • San Francisco, CA, USA

Photovoltaics Technology and Manufacturing

July 13 • San Francisco, CA, USA

Reliability Challenges

July 15 • San Francisco, CA, USA



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Ask the Experts

Q: Is there difference in 2nd level qual between BGA and QFN?

A: Some of the same factors apply, but the packages are very different. Differences include lead free or not, solder process, standoff from board, dimensions, and pitch. QFN is much smaller, is made from different materials, and has a different construction, pitch, aspect ratio, etc. A lot of data is necessary to justify a relationship with much confidence. For more information, please see the following resources:

Paper on the robustness process

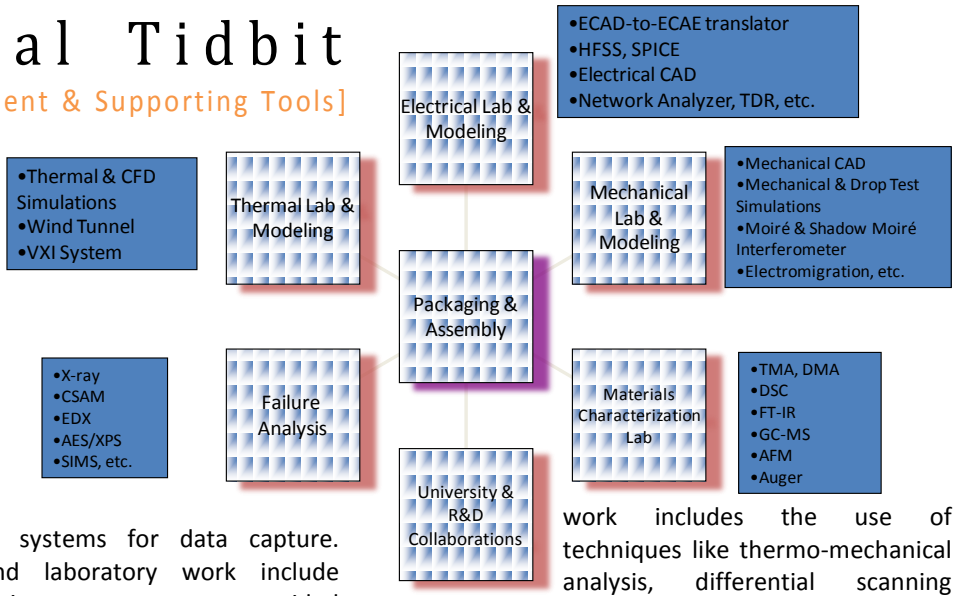
ZVEI link

Spreadsheet template to use in evaluating robustness factors – very complicated

To post, read, or answer a question, visit http://forums.semitracks.com/.
We look forward to hearing from you!

Technical Tidbit

[Package Development & Supporting Tools]



This chart illustrates the package development process and the laboratory and research efforts that support it. Thermal modeling and laboratory work involve tasks such as thermal and computational fluid dynamics simulations, wind tunnel tests, and VXI systems for data capture. Electrical modeling and laboratory work include computer-aided drawing to computer-aided engineering translators, physics modeling through simulators like HFSS, electrical circuit modeling through SPICE simulation, electrical computer-aided design drawings, and laboratory testing using network analyzers, time domain reflectometry, and other tools. Mechanical modeling and laboratory work includes development of mechanical CAD drawings, mechanical and drop test simulations, as well as Moire interferometry measurements for stress and electromigration testing. Materials characterization lab work includes the use of techniques like thermo-mechanical analysis, differential scanning calorimetry, fourier transform infrared spectroscopy, gas chromatograph mass spectroscopy, atomic force micorscopy and Auger electron spectroscopy. Failure analysis lab work includes techniques like radiography, acoustic microscopy, energy dispersive spectroscopy, x-ray photoelectron spectroscopy and secondary ion mass spectroscopy. Further collaborations with universities and national labs may be necessary for new, high-risk development efforts.

RF & Mixed-Signal Testing

[Course Spotlight]

Most new semiconductor applications involve a combination of analog and digital signals that drive actuators, read sensors, and convert these signals into digital data. These applications may also involve wireless signals that transfer data at RF frequencies. As a result, the industry is using an array of mixed-signal components—and facing increasing testing challenges.

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