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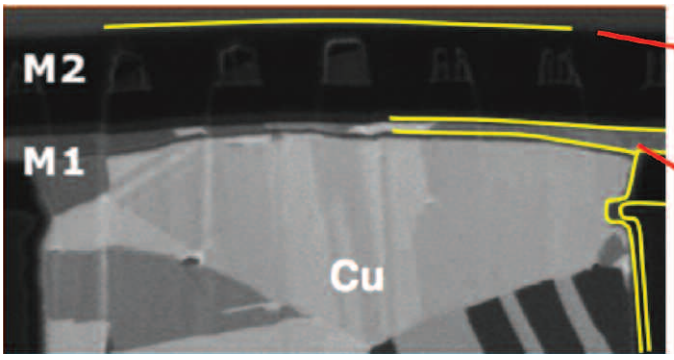
Semitracks Monthly Newsletter

TSV Failure Mechanisms

By Christopher Henderson

This section covers Through-Silicon Via, or TSV, Failure Mechanisms. The first failure mechanism we'll discuss is copper pumping. This is related to the difference in coefficients of thermal expansion between the silicon die and the copper TSV. Thermal stresses cause the copper to expand, putting upward pressure on the the TSV. This stresses the metal and Back End Of Line (BEOL) dielectric layers above and adjacent to the copper TSV structure. This can lead to BEOL failures. Although we can't eliminate the overall stress unless we completely remove the copper, we can lower it by performing annealing and sintering to help lower the overall stress. This image shows an example of the bulging effect associated with copper pumping.

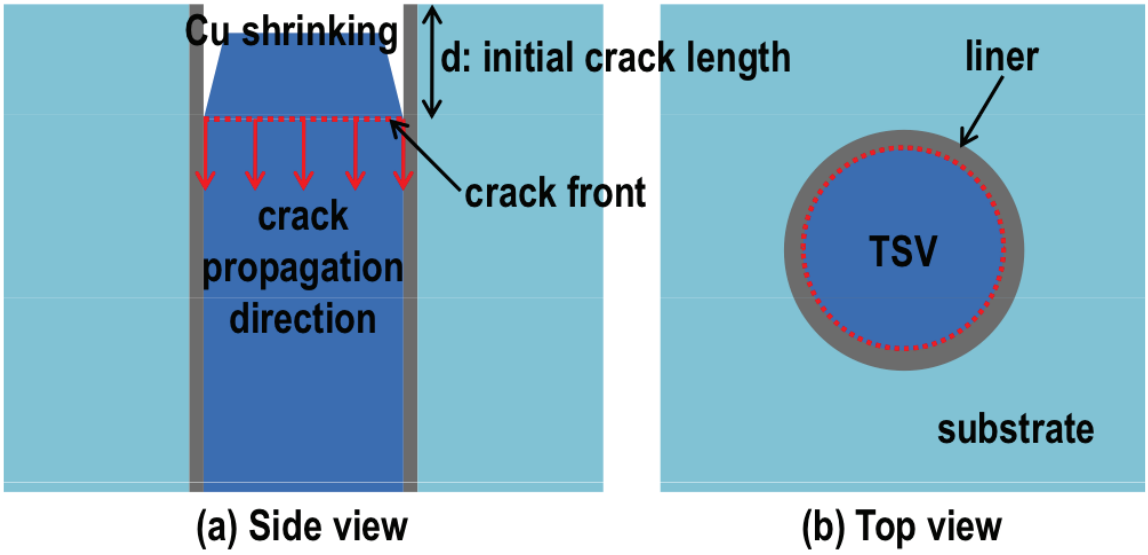


TSV and BEOL bulging after device sintering

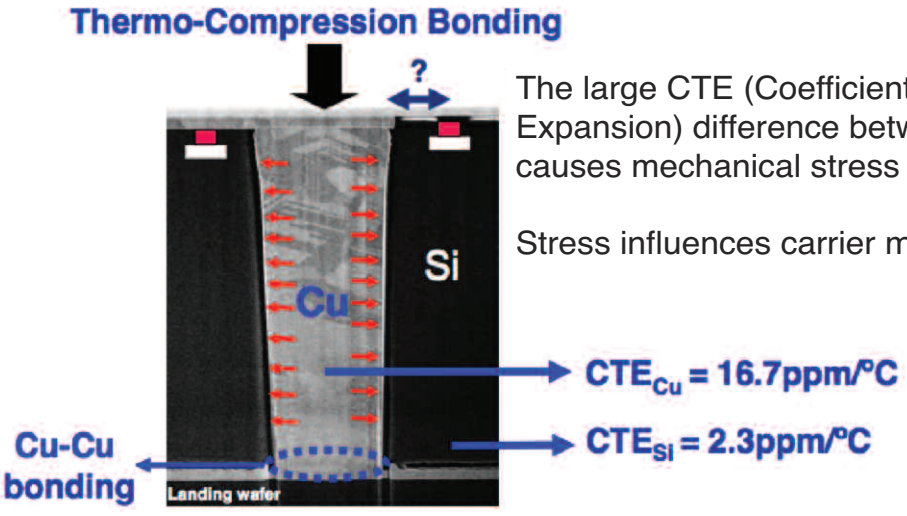
Metal 1 thinner on TSV due to bulging

In this Issue:

Another reliability issue is TSV interfacial cracking. This problem is somewhat the opposite of the copper pumping problem. In this scenario, the copper shrinks back faster than the silicon as one cools down from the TSV deposition temperature. A crack can form around the TSV circumference near the top surface, and then propagate down along the interface between the liner and the TSV. This can result in breaks to the layers connecting to the TSV, such as metal 1.



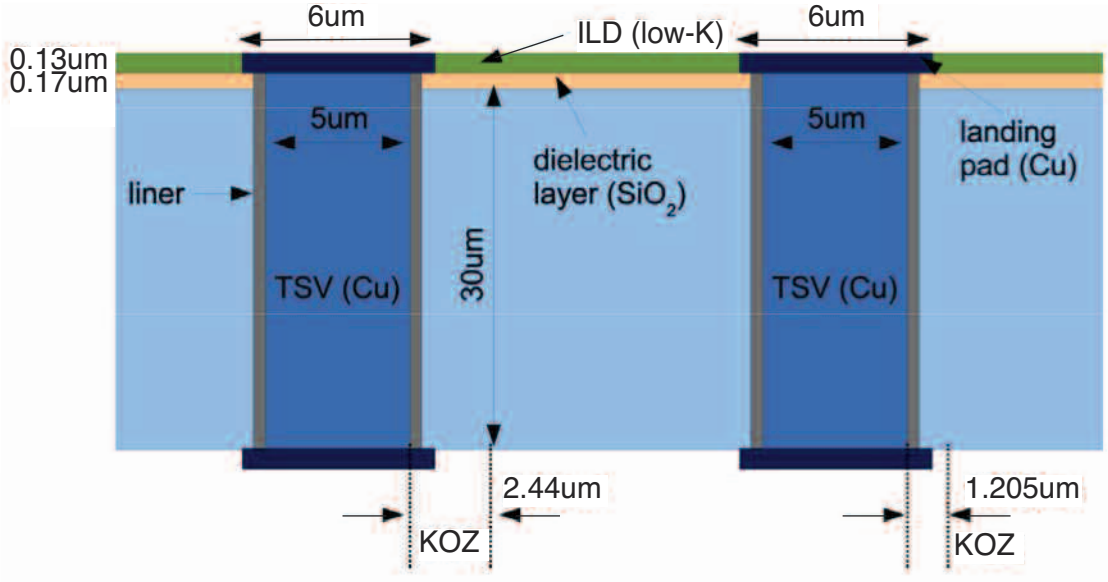
Another problem associated with TSVs is the compressive stress placed on the silicon because of the difference in coefficient of thermal expansion between the silicon and the copper. The stress in the silicon will affect the carrier mobility.



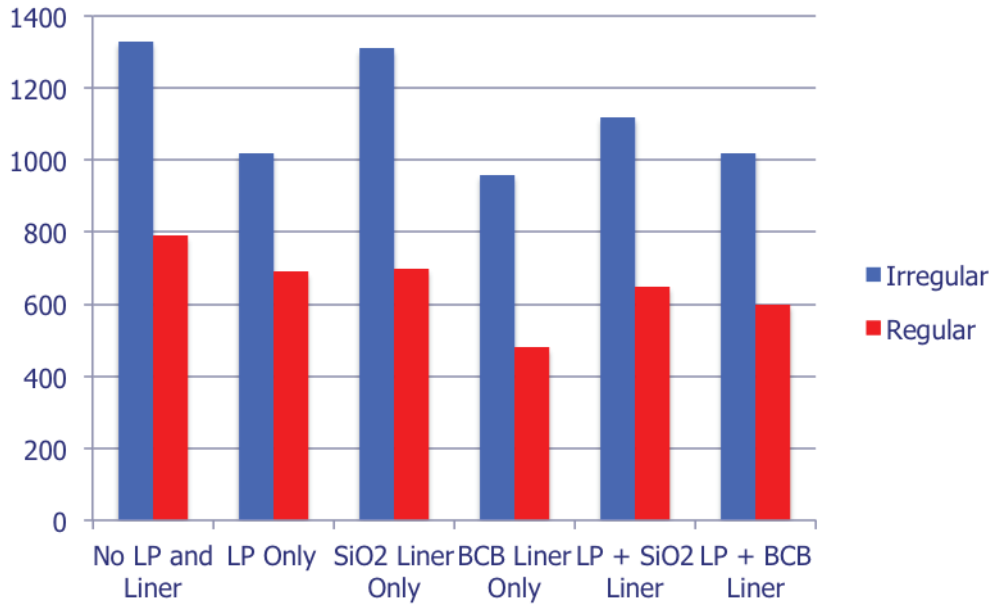
The large CTE (Coefficient of Thermal Expansion) difference between Si and Cu causes mechanical stress in the Si.

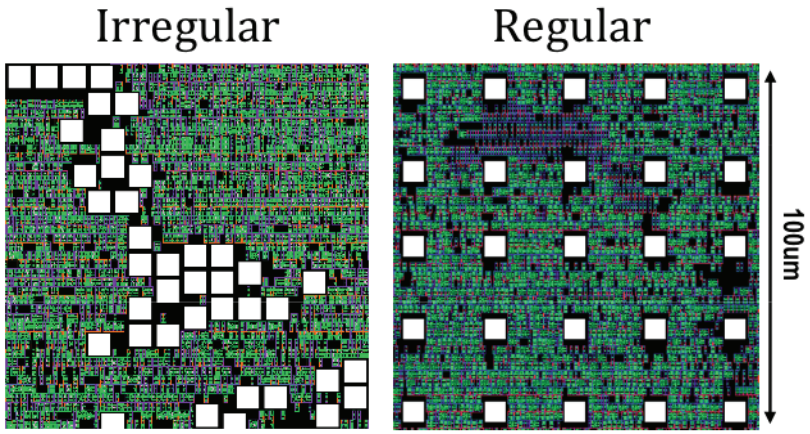
Stress influences carrier mobility.

These stresses must be accounted for during the design phase. One must model the stresses created by the TSV. One must consider the effect of the TSVs together, not just in isolation. Designers need to optimize the TSV placement early in the design process to reduce these mechanical reliability problems. The placement style, keep-out zone sizes, liners, and landings all play a role in the overall behavior of the stress and the effect on the transistors in the circuit.

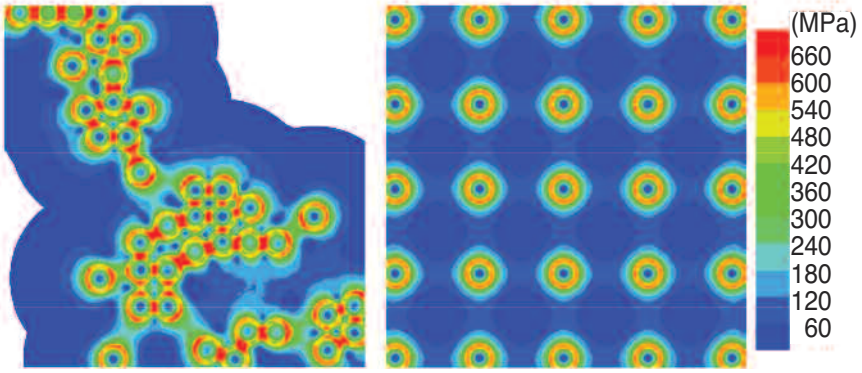


In the figures below, we show the stress in two scenarios: one with the TSVs placed favorably for electrical connections (and irregular pattern from a geometrical standpoint), and TSVs placed favorably to reduce stress (a more uniform geometrical pattern). Notice that the irregular pattern produces higher stresses in all of the material scenarios. The irregular placing also leads to regions of very high stress in localized regions, whereas the regular placing leads to a more uniform amount of stress, with lower peaks but no regions of zero stress.





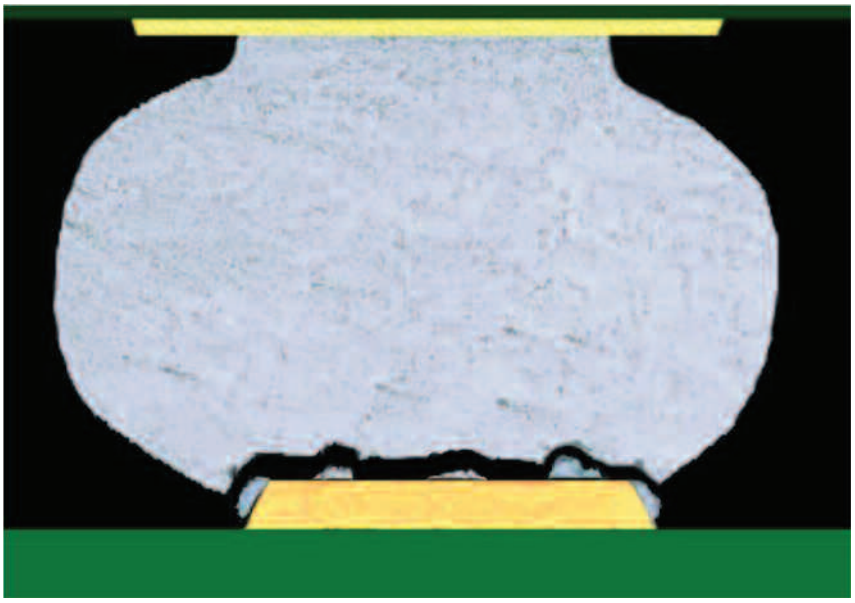
Von Mises map



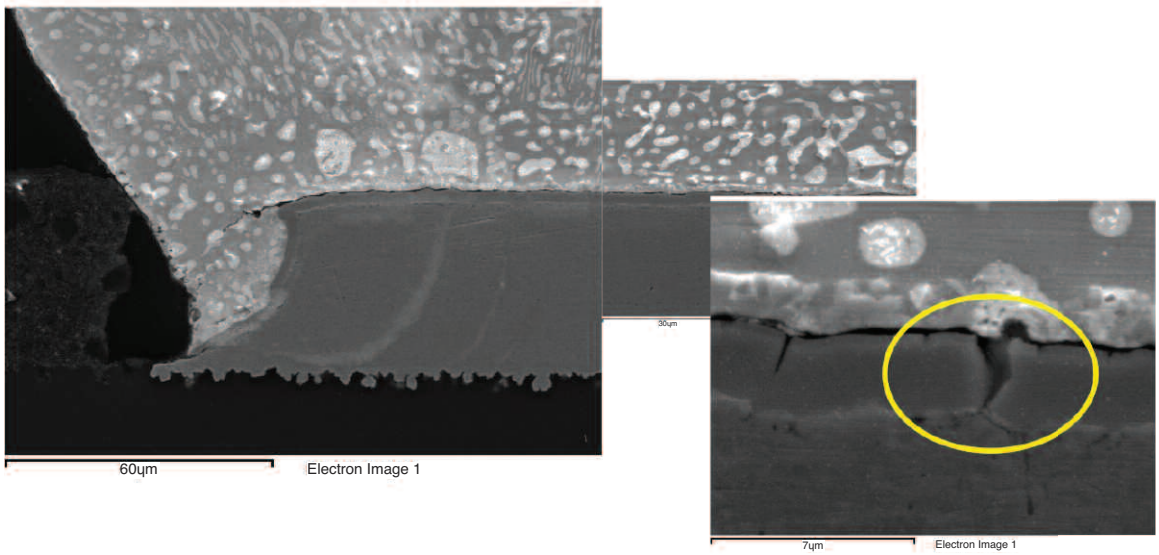
Technical Tidbit

Black Pad

This month's technical tidbit is on a failure mechanism known as Black Pad. It is associated with the electroless-nickel immersion gold surface finishes. Corrosion of the nickel interface layer prevents the solder from properly bonding to the pad, resulting in failures at the solder joint – printed circuit board interface. The pads will typically have a black and grainy appearance, hence the name "black pad." We show a cross-section image of a black pad failure on the right. This problem is particularly difficult because it cannot be detected during the fabrication or assembly stage. The failures typically occur after mechanical stresses like thermal cycling or during use of the product. These failures are most commonly associated with BGA devices, but this problem can also happen with leaded and leadless devices.



Again, the cause of black pad is corrosion of the nickel layer. This creates cracks that reach into the underlying copper layer. Sometimes engineers will refer to this effect as "mud flat cracking". Here we show an SEM cross-section at low magnification on the left, and at high magnification on the right. The cracking is visible here.

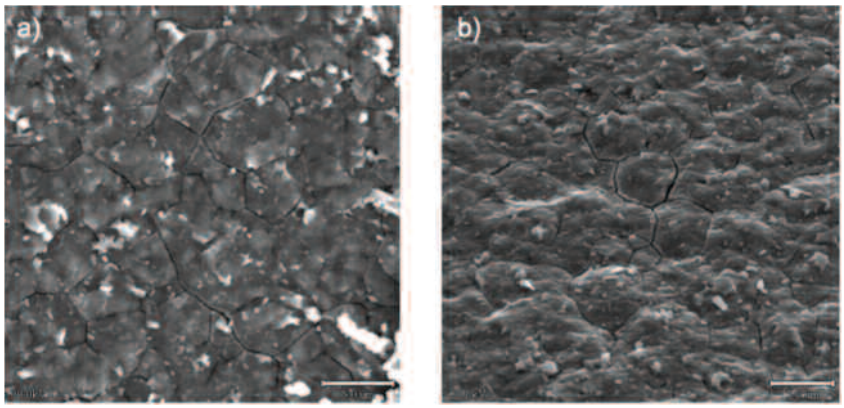


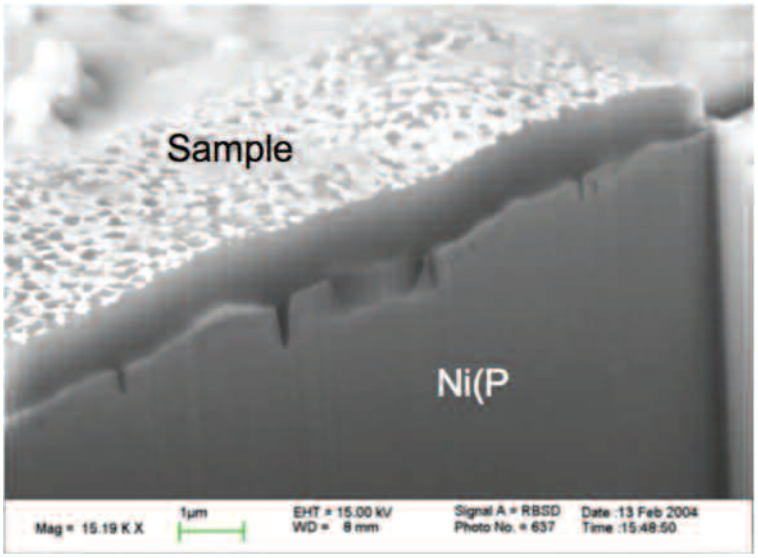
This is a problem that occurs only on Electroless Nickel Immersion Gold, or ENIG (pronounced "e-nig") finishes. ENIG finishes have exhibited the black pad defect that can cause brittle fracture at the interface between solder and metal pad. The failure typically occurs during mechanical or thermal-mechanical testing. The worst cases are BGA package solder joint failures during a customer's surface mount assembly process, or in the product's final use by a consumer.

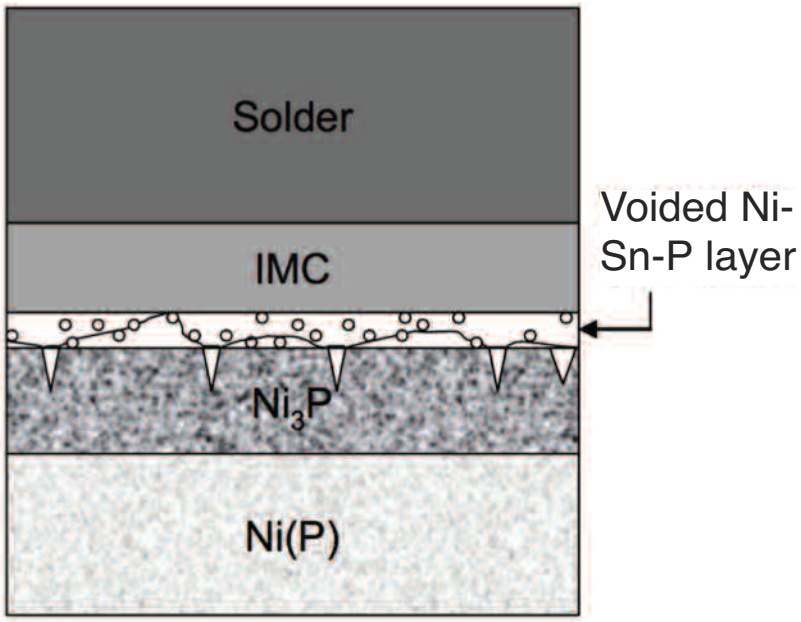
There is consensus as to these factors related to Blackpad:

1. Black pad defects of the ENIG plating are the result of hyperactive corrosion of the Ni(P) (pronounced "nickel-phosphorus") plating by the immersion gold plating bath. The mud-cracks are not created by the soldering process.
2. Formation of the nickel-3 phosphorus layer is the result of crystallization of the amorphous Ni(P) plating assisted by solder reaction. The high phosphorus content of this layer is not by itself evidence for black pad defect.
3. The criteria for black pad failure of solder joints are: 1) flat pad surface, 2) mud-cracks in the pad surface in sample tilt view, and 3) spikes observed in cross section.
4. Interfacial failure of solder joints with ENIG is the combined effect of hyper-galvanic corrosion of Ni(P) during gold plating and Kirkendall voiding in the nickel-3-tin-phosphorus layer after reflow. To avoid the black pad failure of solder joints, the key is to avoid hyper-galvanic corrosion of the Ni(P) plating during gold plating.

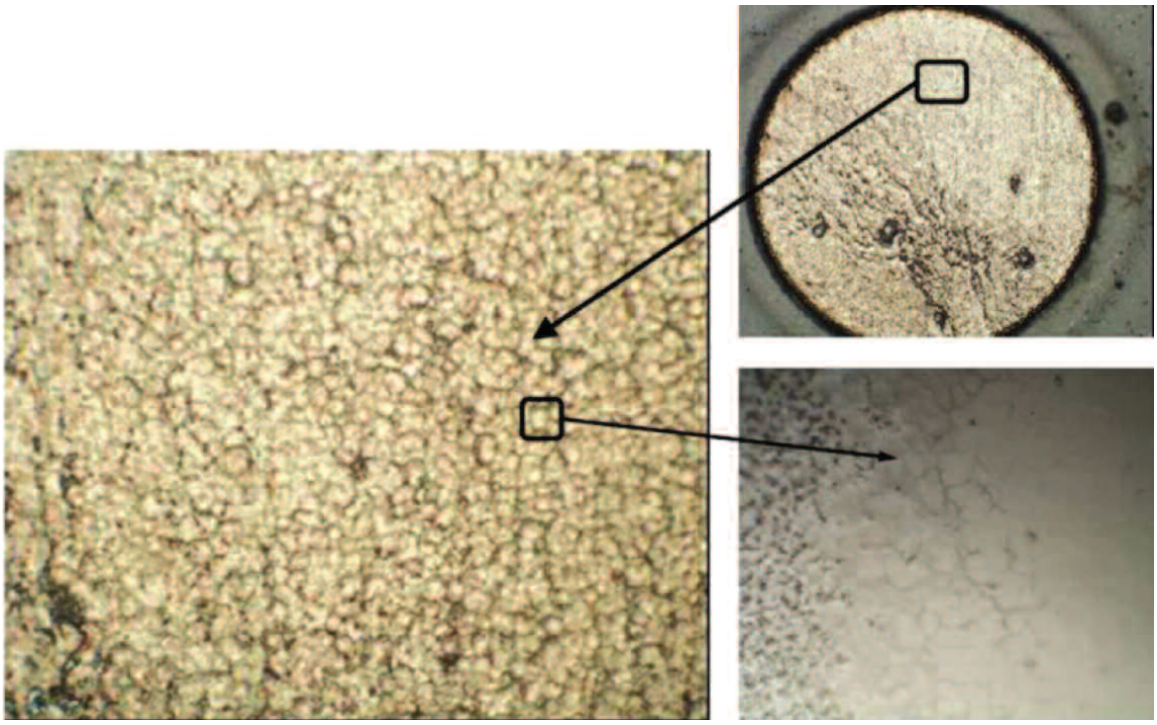
The first figure shows a) Top-view and b) 30-degree-tilt view of black pad mud-cracks in the entire pad surface. The second image shows a cross section through several cracks in large angles and one in parallel. Spikes in cross section is the conclusive evidence for black pad.







Black pad/black nickel can be seen visually. One can use optical techniques to identify the problem and SEM with energy dispersive x-ray analysis to characterize the problem.



Experiments show that lead-free soldering itself does not affect the formation of Black Pad, however, during rework, this phenomenon is more likely to occur. During soldering, formation of black pad can be reduced with thermal considerations and plating parameter optimization. Some thermal considerations for soldering include:

- Minimizing the time above liquidus in the case of reflow soldering, and minimizing the dwell time in wave soldering processes.
- Minimizing the peak temperature
- Optimizing the plating parameters by reducing phosphorus content in nickel bath. A phosphorus content of 11% usually does not typically cause the black pad effect. Generally a minimal phosphorus content of 9.5% is recommended for good corrosion resistance. Assure that the electroless nickel coating is active/solderable prior to applying subsequent protective coatings. Deposit protective gold coating from a minimally corrosive neutral gold bath.

Another possible solution can be the usage of immersion silver coatings instead of nickel gold surface finishes, as this can avoid the failures caused by Black Pad.

Ask the Experts

Q: Hot carrier injection is dominant when the gate voltage is ~ 50% of the power supply voltage. Can this effect couple with NBTI or PBTI which is dominant when the gate voltage is at 0 volts or at the power supply voltage?

A: This is a rather complex issue as both HCI and NBTI have various electric field dependencies. A good place to start to understand this issue is to read "High-VGS PFET DC Hot-Carrier Mechanism and Its Relation to AC Degradation," by Rauch, Guarin, and LaRosa in the March 2010 IEEE TDMR. They developed a model that can help provide some understanding of the interactions involved. You'll need to read additional/newer work as well though, since this is a topic with an understanding that is evolving over time.

Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of wafer fab processing.
5. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Module 1: Basics & Fundamentals; Semiconductor Devices and ICs
    a. Acronyms
    b. Common Terminology
    c. Brief History
    d. Semiconductor Materials
    e. Electrical Conductivity
    f. Semiconductor Devices
    g. Classification of ICs & IC Processes
    h. Integrated Circuit Types
2. Module 2: Crystallinity, Crystal Defects, Crystal Growth
    a. Crystallinity
    b. Crystal Defects
    c. Crystal Growth
    d. Controlling Crystal Defects
3. Module 3: Basic CMOS Process Flow
    a. Transistors and Isolation
    b. Contacts/Vias Formation
    c. Interconnects
    d. Parametric Testing
4. Module 4: Ion Implantation 1 (The Science)
    a. Doping Basics
    b. Ion Implantation Basics
    c. Dopant Profiles
    d. Crystal Damage & Annealing

5. Module 5: Ion Implantation 2 (Equipment, Process Issues)
    a. Equipment
    b. Process Challenges
    c. Process Monitoring & Characterization
    d. New Techniques

Day 2

6. Module 6: Thermal Processing
    a. Overview of Thermal Processing
    b. Process Applications of SiO2
    c. Thermal Oxidation
    d. Thermal Oxidation Reaction Kinetics
    e. Oxide Quality
    f. Atomistic Models of Thermal Diffusion
    g. Thermal Diffusion Kinetics
    h. Thermal Annealing
    i. Thermal Processing Hardware
    j. Process Control
7. Module 7: Contamination Monitoring and Control
    a. Contamination Forms & Effects
    b. Contamination Sources & Control
    c. Contamination Characterization & Measurement
8. Module 8: Wafer Cleaning
    a. Wafer Cleaning Strategies
    b. Chemical Cleaning
    c. Mechanical Cleaning
9. Module 9: Vacuum, Thin Film, & Plasma Basics
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics
10. Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
    a. CVD Basics
    b. LPCVD Films
    c. LPCVD Equipment
    d. Epi Basics
    e. Epi Process Applications
    f. Epi Deposition Process
    g. Epi Deposition Equipment

Day 3

11. Module 11: PVD
    a. PVD (Physical Vapor Deposition) Basics
    b. Sputter Deposition Process
    c. Sputter Deposition Equipment
    d. Al-Based Films
    e. Step Coverage and Contact/Via Hole Filling
    f. Metal Film Evaluation
12. Module 12: Lithography 1 (Photoresist Processing)
    a. Basic Lithography Process
    b. Photoresist Materials
    c. Photoresist Process Flow
    d. Photoresist Processing Systems
13. Module 13: Lithography 2 (Image Formation)
    a. Basic Optics
    b. Imaging
    c. Equipment Overview
    d. Actinic Illumination
    e. Exposure Tools
14. Module 14: Lithgroaphy 3 (Registration, Photomasks, RETs)
    a. Registration
    b. Photomasks
    c. Resolution Enhancement Techniques
    d. The Evolution of Optical Lithography
15. Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
    a. Etch Basics
    b. Etch Terminology
    c. Wet Etch Overview
    d. Wet Etch Chemistries
    e. Types of Dry Etch Processes
    f. Physics & Chemistry of Plasma Etching

Day 4

16. Module 16: Etch 2 (Dry Etch Applications and Equipment)
    a. Dry Etch Applications
    b. SiO2
    c. Polysilicon
    d. Al & Al Alloys
    e. Photoresist Strip
    f. Silicon Nitride
    g. Dry Etch Equipment
    h. Batch Etchers
    i. Single Wafer Etchers
    j. Endpoint Detection
    k. Wafer Chucks
17. Module 17: CVD 2 (PECVD)
    a. CVD Basics
    b. PECVD Equipment
    c. CVD Films
    d. Step Coverage
18. Module 18: Chemical Mechanical Polishing
    a. Planarization Basics
    b. CMP Basics
    c. CMP Processes
    d. Process Challenges
    e. Equipment
    f. Process Control
19. Module 19: Copper Interconnect, Low-k Dielectrics
    a. Limitations of "Conventional" Interconnect
    b. Copper Interconnect
    c. Cu Electroplating
    d. Damascene Structures
    e. Low-k IMDs
    f. Cleaning Cu and low-k IMDs

20. Module 20: Leading Edge Technologies & Techniques
    a. Process Evolution
    b. Atomic Layer Deposition (ALD)
    c. High-k Gate and Capacitor Dielectrics
    d. Ni Silicide Contacts
    e. Metal Gates
    f. Silicon on Insulator (SOI) Technology
    g. Strained Silicon
    h. Hard Mask Trim Etch
    i. New Doping Techniques
    j. New Annealing Techniques
    k. Other New Techniques
    l. Summary of Industry Trends

References:

Wolf, Microchip Manufacturing,
Doering & Nishi, Semiconductor Manufacturing Technology, 2nd ed.
Wolf, Silicon Processing, Vol. 4
Wolf, Silicon Processing, Vol. 1, 2nd ed.

DESIGN AUTOMATION CONFERENCE 54

2017 Design Automation Conference

June 18-22, 2017
Austin Convention Center
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Austin, TX, USA 78701

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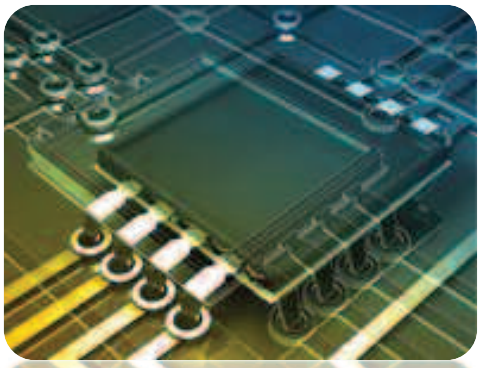
Semitracks will be at the Si2.org booth, and would be happy to discuss training needs, and creating training materials for your userbase.
Contact us at info@semitracks.com during the conference!



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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

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Upcoming Courses

(Click on each item for details)

Semiconductor Reliability and Qualification
May 15 – 18, 2017 (Mon – Thur)
Munich, Germany

Semiconductor Statistics
May 22 – 23, 2017 (Mon – Tue)
Munich, Germany

Wafer Fab Processing
June 5 – 8, 2017 (Mon – Thur)
Portland, Oregon, USA