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Semitracks Monthly Newsletter

Basic Failure Mechanisms

By Christopher Henderson

This month, we begin a new series of Feature Articles that will cover Failure Mechanisms. While there are literally hundreds of semiconductor and integrated circuit-related failure mechanisms, there are some common ones of which you should be aware. Over the next four Feature Articles, we will cover these basic failure mechanisms: Particles and Defects, Die Reliability-Related Failure Mechanisms, Package-Related Failure Mechanisms, and Use Condition Failure Mechanisms. We begin this month with Particles and Defects.

Particles and Defects

Defects are one of the more important concerns to the manufacturing staff in a semiconductor manufacturing plant. Defects can be introduced from a wide variety of sources. These sources include the wafer processing equipment, the chemicals and gases used during processing, wafer handling, and a host of other sources. These defects will have a distribution that covers a wide range of sizes and types. Process and yield engineers have consistently observed that the number of particles increases as the size of the particle decreases. Therefore, fewer large particles make it to the wafer surface, while more smaller particles do. Particles that land on the wafer surface can create defects during processing that can cause the chip to fail.

In this Issue:

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An obvious aspect of defects is that they reduce yields on semiconductor components. Let's use the following example to illustrate this point. Let's assume that we have patterned an integrated circuit such that it has a number of parallel interconnect segments, as shown in Figure 1. This situation could occur on a number of different metal layers in the circuit. Let's now assume we have some defects on the circuit as well. The bigger defects, shown on the left of Figure 1, would cause the circuit to function incorrectly. A large non-conductive particle would cause an open on one or more interconnects, while a large conductive particle would cause a short circuit between two or more interconnects. The defects in the center of Figure 1 may or may not cause a functional problem. Their ability to create a functional error in the circuit would be dependent on their exact placement. The particles on the right of Figure 1 would most likely not cause a functional problem because they are too small to bridge two lines or cause an open on a line.

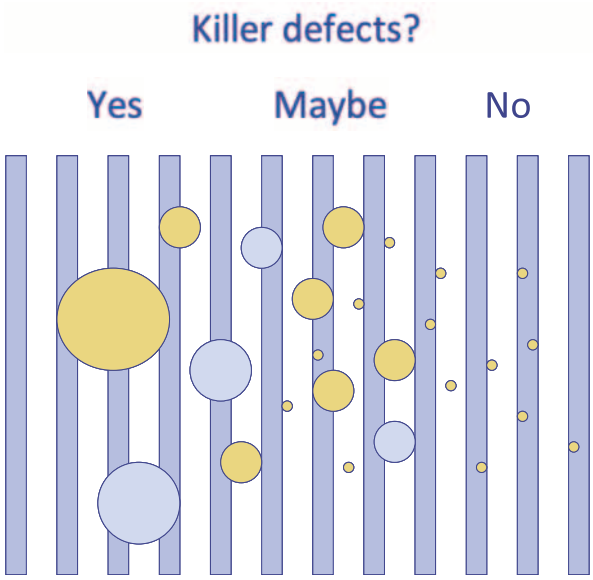


Figure 1. Defect size distribution and its effect on IC operation.

Defects can be classified into several major groups:

- Bulk silicon or crystalline defects
- Patterning defects
- Particle defects
- Workmanship defects

We will examine each one of these defects and their effects on semiconductor failures.

Bulk Silicon (Crystalline) Defects

A common failure mechanism early in the semiconductor industry was the silicon defect. Manufacturers used the Czochralski method to grow wafers, but this process would introduce defects if not controlled precisely. This would include problems like oxygen defects, impurities, and crystalline

structure defects. Subsequent wafer processing also caused defects. As shown in Figure 2, the thermal processes associated with oxidation, diffusion, and/or implant annealing caused stacking faults in the silicon. These can be seen as shaded vertical ellipses in the optical interference contrast image. The stress in the oxide causes a polarization change that produces contrast in the image.

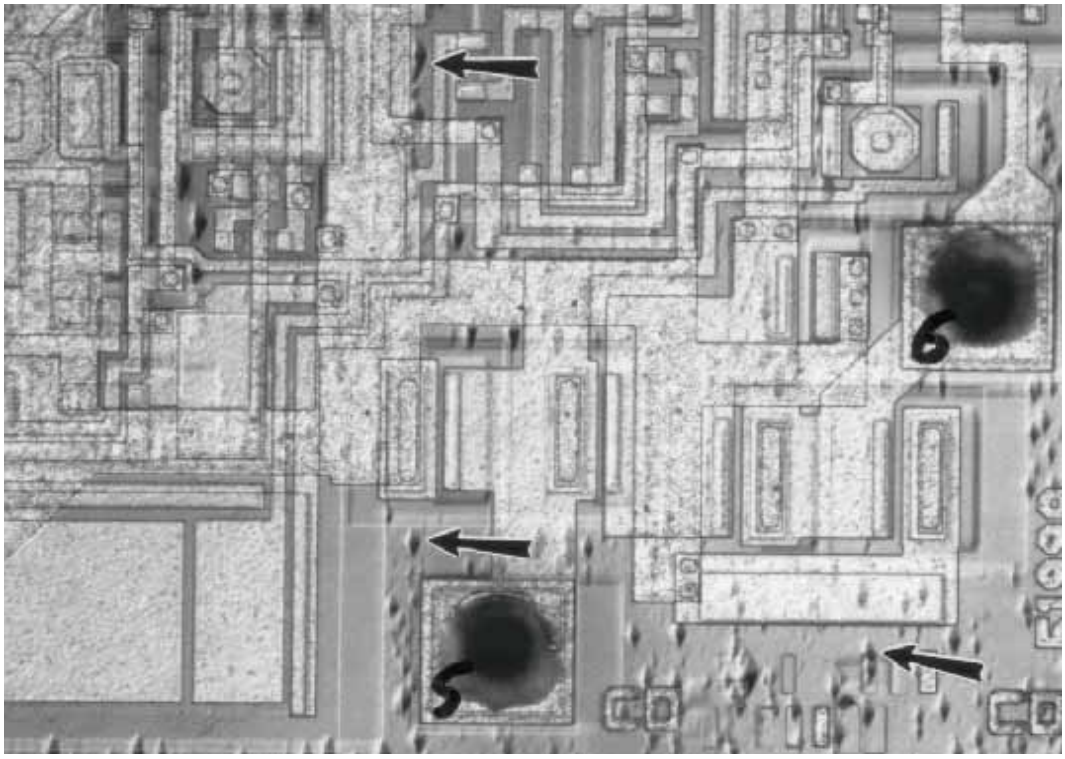
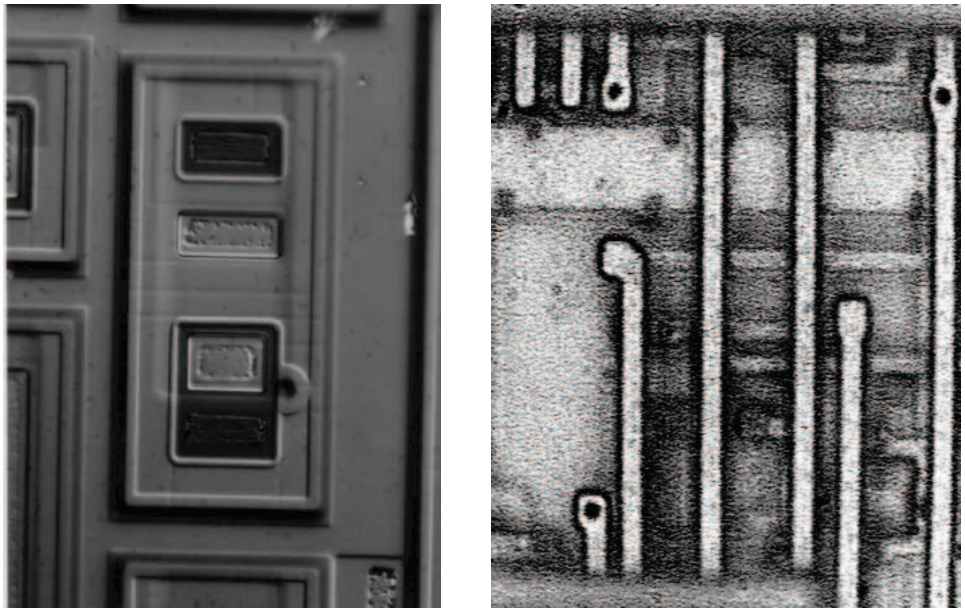


Figure 2. Stacking faults (Image courtesy Phillips Semiconductors).

Patterning Defects

Particles or contamination on the wafer or on the reticle can cause patterning defects on the integrated circuit. Figure 3 shows two such cases. The image in Figure 3(a) shows the results of a particle that was present on the wafer or the reticle during the base diffusion patterning step. The image in Figure 3(b) shows two vias missing that should connect metal-2 to metal-3. A particle or contamination on the reticle in this area prevented the vias from being patterned.



(a) (b)

Figure 3. (a) Defect at base diffusion and (b) defect at metal-1/metal-2 via.

Particle Defects

Particles can also land directly on the wafer and create problems. The image in Figure 4 shows an example of a particle with a significant amount of tungsten embedded in it. This created a leakage path between the power and ground connections (the thicker metal interconnect runs vertically in the image).

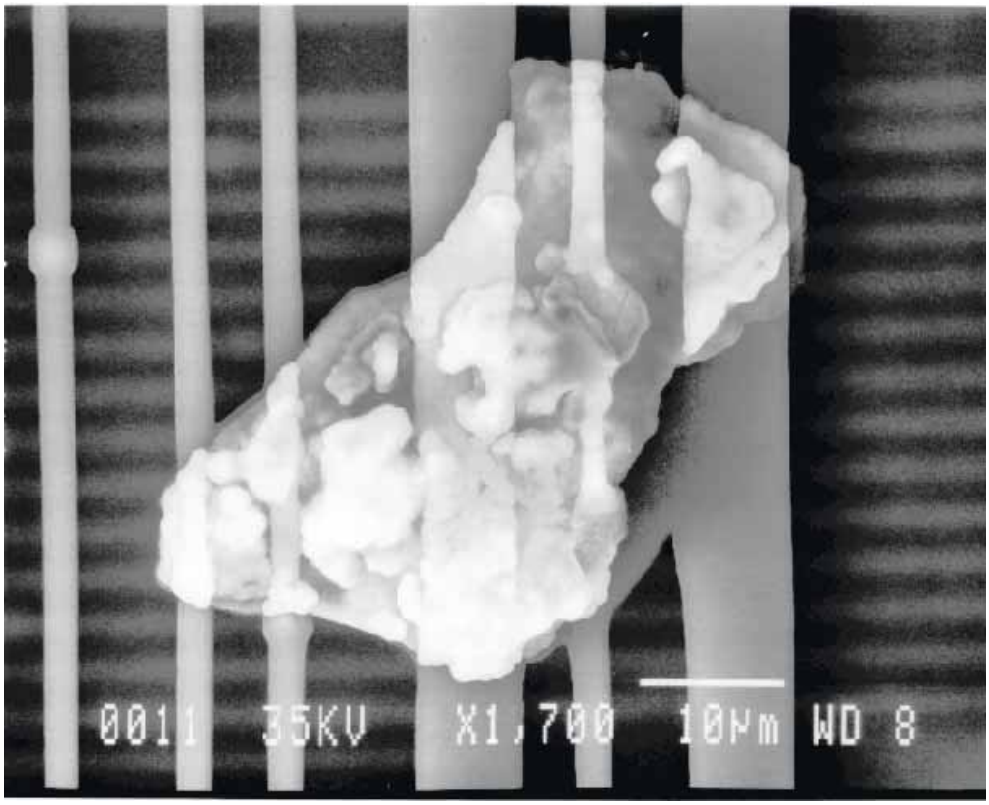
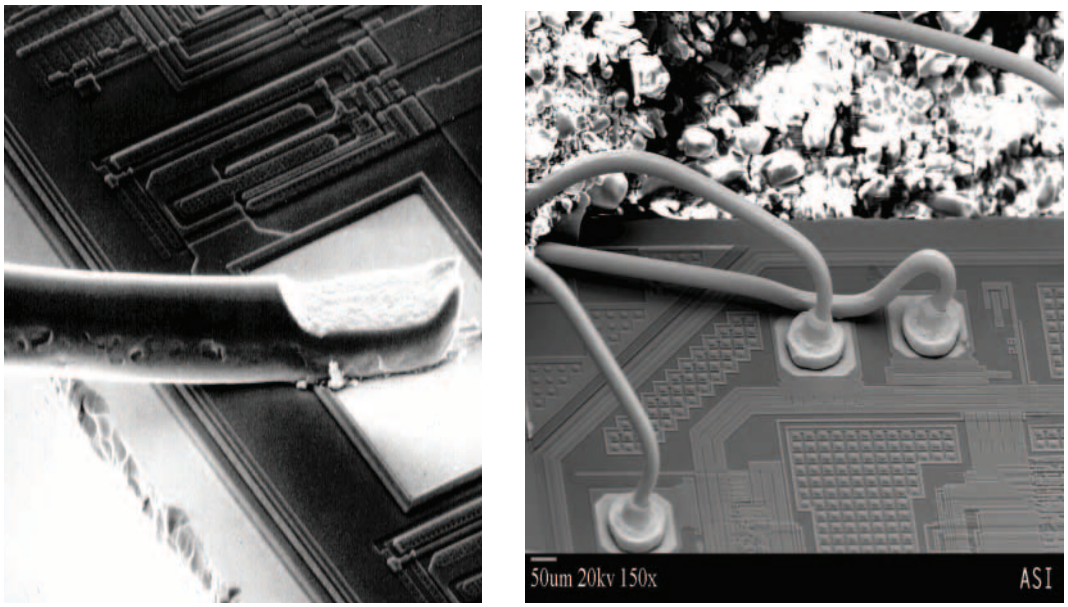


Figure 4. Results of a tungsten particle at metal-3 patterning.

Workmanship Defects

A whole host of problems can occur at the packaging level due to workmanship problems. In Figure 5 we show two examples. The image in Figure 5(a) shows an aluminum bond wire with a low takeoff angle. This low angle led to a small gap between the edge of the die where a conductive particle could short the bond wire to the scribe line. The image in Figure 5(b) shows gold bond wires that were smashed down by either human handling or improper machine operation. The good news is that these defects are less common today. Automation of the assembly/test process leads to less workmanship defects in general. However, assembly/test involves more significant human handling and non-standard procedures, given the enormous number of semiconductor and integrated circuit package configurations produced today.



(a) (b)

Figure 5. (a)Wire bond to chip edge clearance and
(b) Assembly-related bond wire short caused by pre-molding mechanical damage.

Process Variation

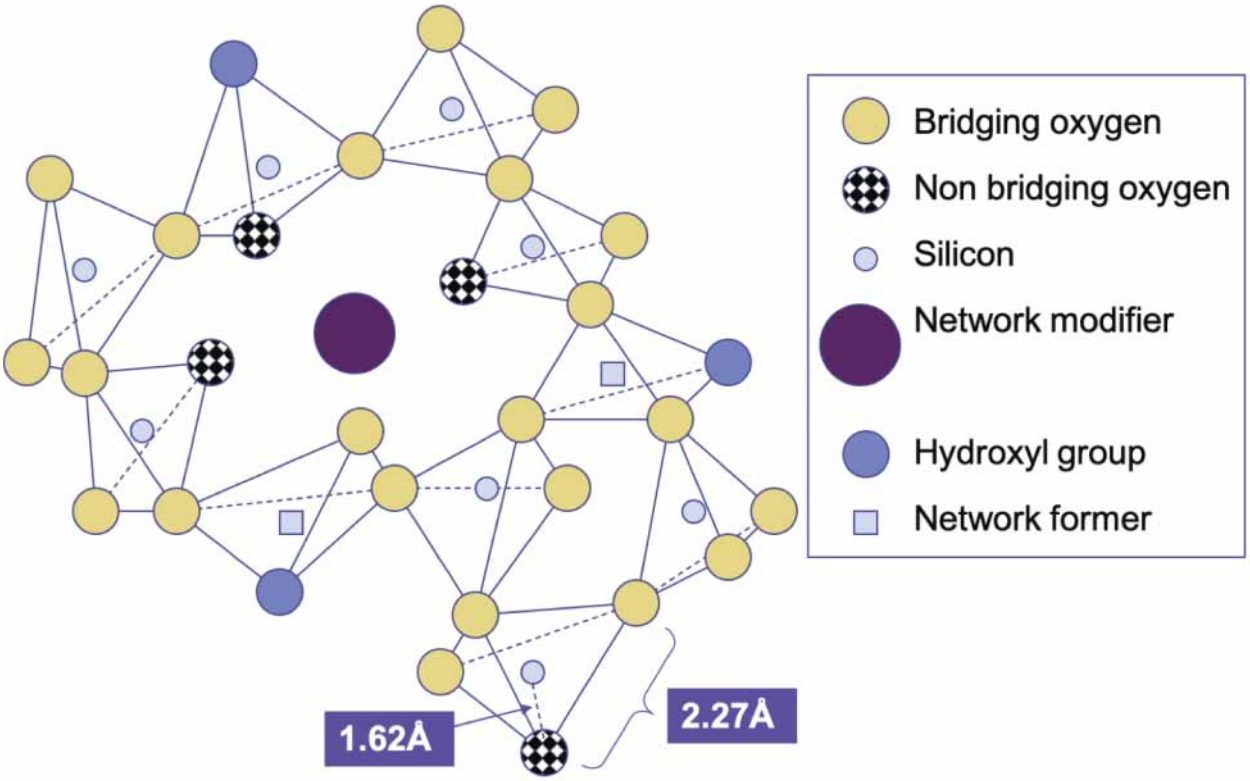
In today's ICs, another big concern is related to process variation. As engineers continue to scale the feature sizes in today's ICs, the ability to control variation in the process has not scaled at the same rate as the feature sizes themselves. Furthermore, some aspects of the process, like oxide thickness, have probably reached the limit in terms of process variation control. Process variation leads to conditions where the individual transistors, metal segments, contacts, vias and other features do not behave the same from one IC to the next, or even across the same IC. These problems can lead to the failure of devices, not only at wafer probe, but also later on during packaging, and even during field use.

In next month's Feature Article, we will cover Die Reliability-Related Failure Mechanisms.

Technical Tidbit

Silicon Dioxide

This month's Technical Tidbit is on one of the most common materials used in semiconductor manufacturing, silicon dioxide.



The glass or amorphous state of silicon dioxide is called fused silica. This state is not thermally stable below about 1700°C. This means that it will slowly convert into a crystalline form. The good news is that this process is so slow below 1000°C that for all intents and purposes, it does not occur. The structure of fused silica glass is moderately complex, as evidenced by the image shown above. Basically, the structure is composed of units of one silicon atom and four oxygen atoms loosely bound together by the oxygen atoms. There are bridging and non-bridging oxygen atoms in the structure. The distance between the silicon atom and the oxygen atoms is 1.62Å, while the distance between oxygen atoms is 2.27Å. The network formers are the doping species like phosphorus and boron. Network modifiers are the mobile ionic species like sodium, potassium, and lead. Because this structure is quite loose, various deposition conditions can lead to various properties. Because of this, process engineers must fine-tune their deposition processes to produce silicon dioxide that exhibits the properties needed for the application, such as dielectric breakdown strength, dielectric constant, stress, resistance to moisture, and resistance to mobile ion penetration.

Ask the Experts

Q: I am doing a Qualification By Similarity (QBS). The product is a new design that is a redesign (an improvement) of an existing design. The silicon technology is the same for the new design as it is for the existing design, and the package and packaging process is the same for the new design as it is for the existing design. Do I need to perform Temperature Cycling as part of my qualification activities?

A: The answer is not completely straightforward. If the re-designed die is smaller, then in theory it would not need to be done. However, if the die size is larger, then the thermomechanical stresses would potentially be higher, so temperature cycling would be recommended as a qualification test. However, even if the die is smaller, some customers may require temperature cycling as a routine qualification test, simply to understand if there is the possibility that thermomechanical stress can cause failures.

Spotlight: Advanced CMOS/FinFET Fabrication

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" Advanced CMOS/ FinFET Fabrication is a 1-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

WHAT WILL I LEARN BY TAKING THIS CLASS

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs and FD-SOI are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including ion implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.
2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.
3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.
4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

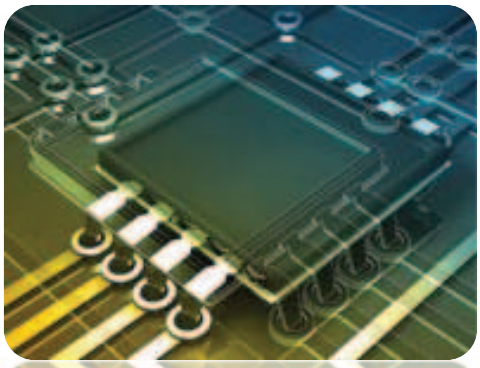
1. The seminar will provide participants with an in-depth understanding of SOI technology and the technical issues.
2. Participants will understand how Hi-K/Metal Gate devices are manufactured.
3. Participants will also understand how FinFET devices are manufactured.

4. The seminar provides a look into the latest challenges with copper metallization and Low-k dielectrics.
5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.
6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.
7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.
8. Finally, the participants see a comparison between FD-SOI (the leading alternative) and FinFETs.

COURSE OUTLINE

1. Advanced CMOS Fabrication – Introduction
2. Front End Of Line (FEOL) Processing
    a. SOI and FD-SOI
    b. Ion Implantation and Rapid Thermal Annealing
    c. Pulsed Plasma Doping
    d. Hi-K/Metal Gates
    e. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
3. Back End Of Line (BEOL) Processing
    a. Introduction and Performance Issues
    b. Copper
        i. Deposition Methods
        ii. Liners
        iii. Capping Materials
        iv. Damascene Processing Steps
    c. Lo-k Dielectrics
        i. Materials
        ii. Processing Methods
    d. Reliability Issues
4. FinFET Manufacturing Overview
    a. Substrates
        i. Bulk
        ii. SOI
    b. FinFET Types
    c. Process Sequence
    d. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology

5. FinFET Reliability
   a. Defect density issues
   b. Gate Stack
   c. Transistor Reliability (BTI and Hot Carriers)
   d. Heat dissipation issues
   e. Failure analysis challenges
6. Future Directions for FinFETs
   a. Comparison of FD-SOI and FinFETs – Are FinFETs a better choice?
   b. Scaling



Upcoming Webinars

(Click on each item for details)

Advanced CMOS/FinFET Fabrication

4 sessions of 2 hours each
US: May 25 – 28, 2021 (Tue – Fri),
8:00 A.M. – 10:00 A.M. PDT

IC Packaging Technology

4 sessions of 4 hours each
SE Asia: June 8 – 11, 2021 (Tue – Fri)
9:00 A.M. – 1:00 P.M. SE Asia Time)

Semiconductor Reliability / Product Qualification

4 sessions of 4 hours each
Europe: August 30 – September 2, 2021
(Mon – Thur), 1:00 P.M. – 5:00 P.M. CET

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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We look forward to hearing from you!