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# InfoTracks

Semitracks Monthly Newsletter

## Thermal Processing—Part IV, Equipment and Processing

By Christopher Henderson

Last month, we delved a little deeper into Thermal Processing, covering Oxidation and Kinetics. This month we'll focus on the equipment and processing used for thermal processes. Basically, thermal processing occurs in furnaces; however, newer thermal annealing techniques use alternate heating techniques like flash lamps and lasers.

The first item to discuss is thermal oxidation hardware. The atmospheric oxidation furnace is the most common hardware used in the industry on legacy wafer sizes of 200mm or less. This technology uses batch processing, where one to two hundred wafers are loaded into the system at once. The hot wall reactor is the most common type, where the reaction chamber is a large silica tube. The entire chamber sits at equilibrium in a hot wall reactor. These systems can be oriented both horizontally and vertically. Vertical orientation tends to be more common today. There is a gas inlet at one end for steam, oxygen, or chlorine-based gases, and an exhaust port at the other end. Engineers design the tube to be surrounded by high-resistance ceramic coils that serve as heating elements. The coils then heat the wafers through conduction and convection processes. The wafers sit in quartz boats that are made of silica similar to the chamber walls. Thermocouples monitor the temperature and proportional–integral–derivative controllers maintain the temperature.

At 300 millimeter wafer sizes, there are some significant issues

## In this Issue:



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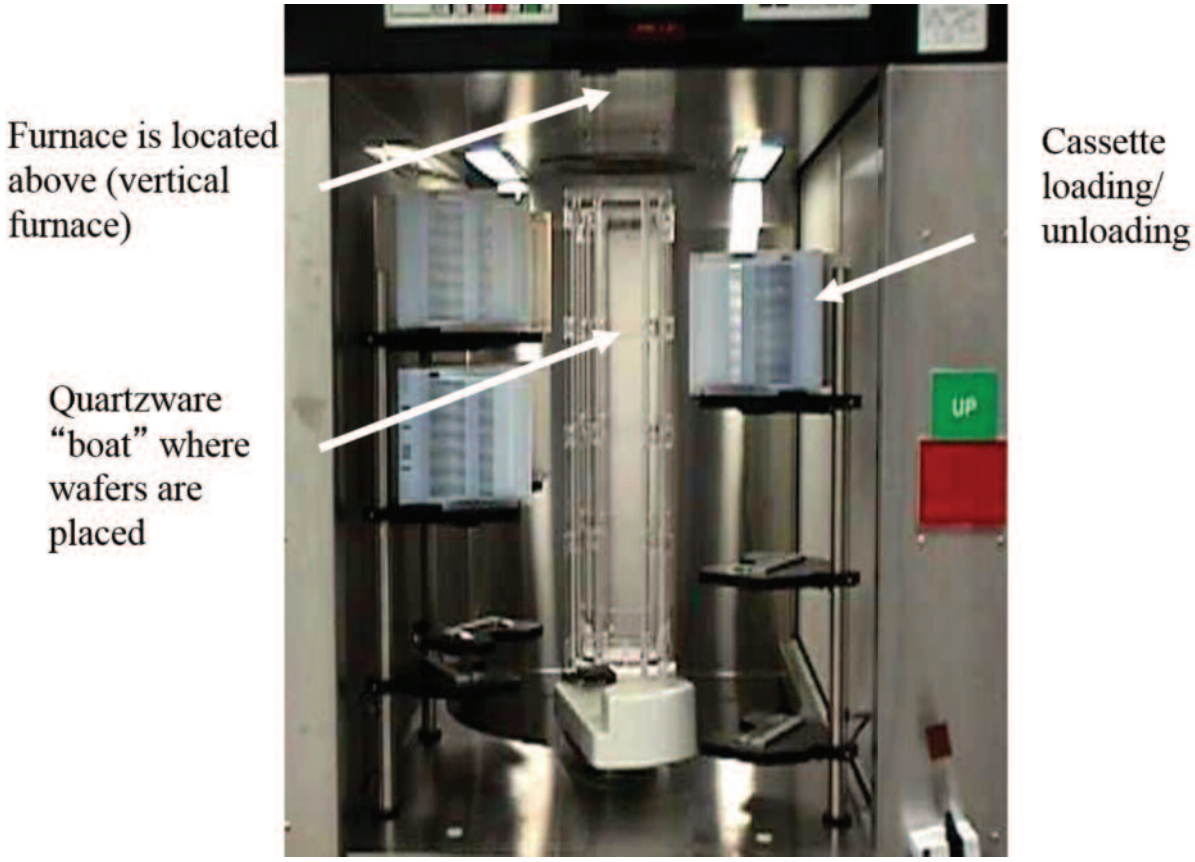
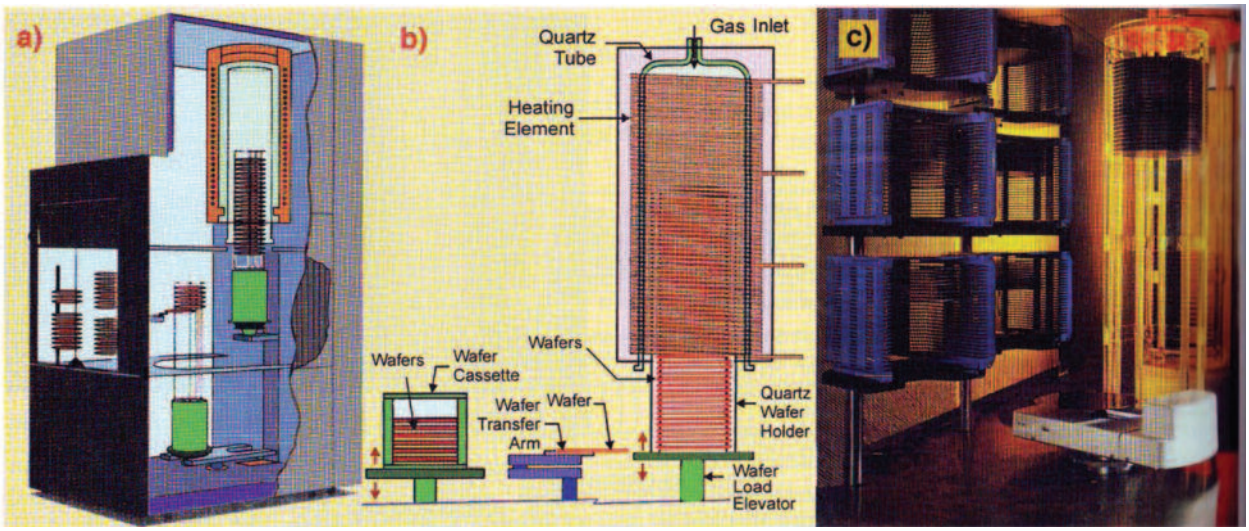
with thermal processing. One problem is the longer thermal lag time and larger thermal masses of the systems and wafers. The wafers will warm more slowly than the environment, leading to skewed thermal profiles. This can lead to problems with dopant redistribution, cross-wafer and cross-batch variabilities, and longer diffusion and oxidation times at lower temperatures. 300 millimeter wafers contain a lot of product dice, so mis-processing at 300mm batch can lead to significant scrap. Most oxidization and diffusion steps cannot be re-worked like deposition steps, so this is a big concern. These tools can take up a lot of room, so it can drive up the cost of the clean room facility. Finally, the size of the wafers and the systems makes tool clustering impractical.

This picture shows a process technician with a boat of wafers in front of an oxidation furnace. This particular system is a vertical furnace. The furnace tube is indicated by the arrow. The yellowish glow indicates that the system is probably at the oxidation temperature.

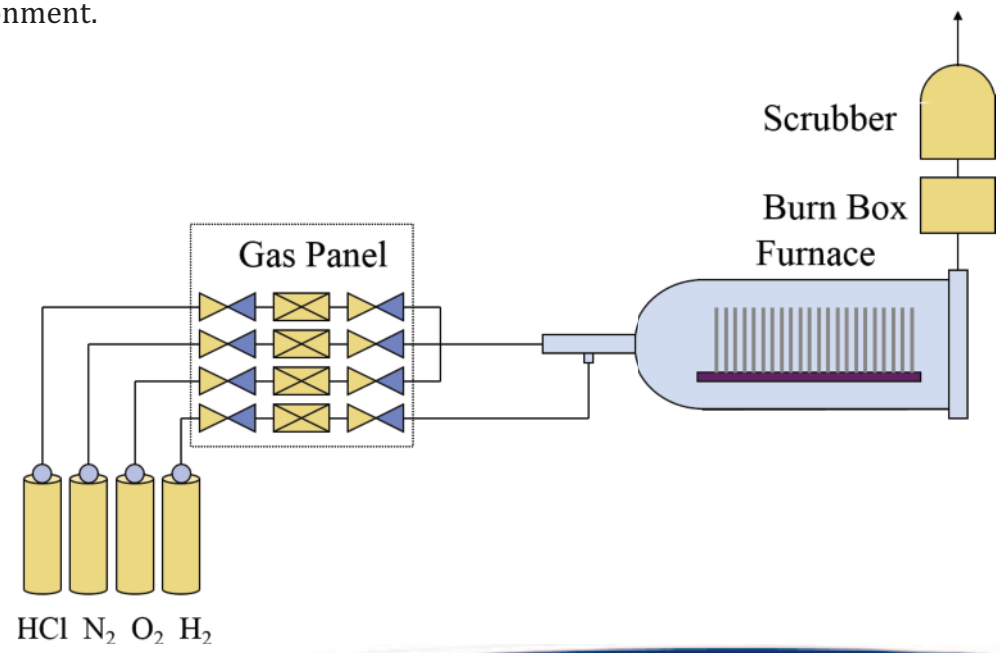
This image shows an example of an oxidation furnace. This particular furnace is a vertical furnace. Most furnaces manufactured today are vertical furnaces, since the temperature profiles can be more easily controlled. Vertical furnaces also take up less room inside the clean room. Given the high cost of clean room space, this makes the vertical furnace the preferred tool. The quartzware rack where the wafers sit during the oxidation process is indicated by the arrow shown here. The quartzware is often referred to as a boat, since it is shaped much like a boat hull. The cassette mechanism for loading and unloading wafers is indicated by the arrow shown here. The cassettes are normally made from a material that does not easily generate particles, like Teflon.



This is an example of an atmospheric oxidation furnace. Many manufacturers use mini-batch reactors for 300 millimeter wafers to reduce the negative side effects we mentioned in the previous slide. Mini batch reactors use a smaller batch size of 25 to 50 wafers along with in-situ rotation to accomplish the thermal process with less risk of large-scale damage. The image on the left shows a cutaway drawing of a vertical furnace, the center image shows a schematic of the loading system, and the image on the right shows an image of a vertical furnace tube.



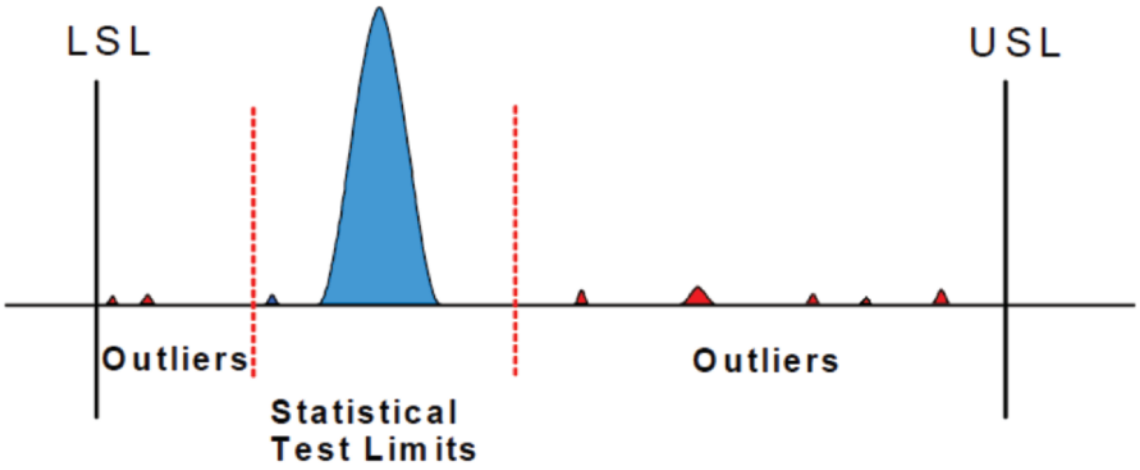

This diagram shows the basic schematic for an oxidation system. Various gases are routed through a gas panel into the oxidation furnace. This allows one to use dry oxygen, hydrochloric acid, and hydrogen in the oxidation environment. One can also use nitrogen to purge the system. The exhaust from the furnace goes through a burn box. The burn box operates at temperatures high enough to oxidize the remaining gases so that they do not present a hazard. The scrubber then removes any toxic chemicals from the environment.



# Technical Tidbit

## Outlier Screening

An outlier is a product that meets the manufacturer specifications and user requirements but exhibits anomalous characteristics with respect to a normal population.




Graphical representation of statistical test limits and outliers

The blue region corresponds to the main portion of the population, while the red data corresponds to the outliers. Outliers can be a problem because some is different with respect to these devices, causing them to fall outside the normal distribution. There is significant evidence from failure and yield analysis work that outliers can then degrade and drift outside the limits set by the product engineers in the product specification. Therefore, it makes sense to eliminate these parts before shipping them. One can use different variables to identify outliers: parametric values associated with transistors, bin data associated with failure modes, continuity/shorts data and overall wafer yield values. Outlier programs can be implemented at parametric test, wafer sort, and at final test. JEDEC Standard JESD50B-01 defines how to run an outlier program, but it does not prescribe how to do the statistical analysis. Most companies will use one or a combination of the following algorithms: the Tukey algorithm, the Cpkn algorithm or the 3 Sigma algorithm to set statistical limits to identify outliers (represented by the dashed red lines in the figure). There are other criteria applied to the identification and disposition of these parts. For more details, see the Outlier Section in the Test or Reliability workspaces on the Online Training Website.

## Ask the Experts

**Q: I think IDDQ would be a useful test for us to be able to localize defects, but the IDDQ defect distribution lies within the main population and is difficult to separate out. Do you have any ideas?**

**A:** You might try using other parameters like temperature and voltage to try and separate the defects out of the population. For instance, you can plot the distribution of IDDQ at 25C against the distribution at 85C, or plot the distribution of IDDQ at 1.5V against the distribution at 2.0V and look for outliers that way.

# Spotlight: Wafer Fab Processing

## OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a one-day course that offers an overview look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we summarize the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

## COURSE OBJECTIVES

1. The seminar will provide participants with an overview of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

5. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
6. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

## INSTRUCTIONAL STRATEGY

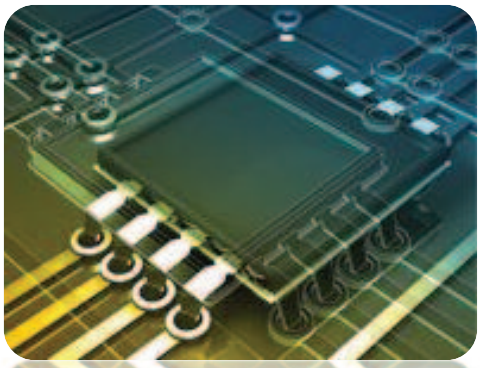
By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

## COURSE OUTLINE

1. Raw Silicon Wafers
2. Ion Implantation
3. Thermal Processing
4. Contamination Monitoring and Control
5. Wafer Cleaning and Surface Preparation
6. Chemical Vapor Deposition
7. Physical Vapor Deposition
8. Lithography
9. Etch
10. Chemical Mechanical Polishing
11. Cu Interconnect and low-k Dielectrics
12. Leading Edge Technologies and Techniques
    a. ALD
    b. high-k gate and capacitor dielectrics
    c. metal gates
    d. SOI
    e. strained silicon
    f. plasma doping

For each of these modules, the following topics will be addressed:

1 fundamentals necessary for a basic understanding of the technique
2 its role(s) and importance in contemporary wafer fab processes
3 type of equipment used
4 challenges
5 trends



# Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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http://www.semitracks.com

*To post, read, or answer a question, visit our forums.*
*We look forward to hearing from you!*

# Upcoming Courses

(Click on each item for details)

### Product Qualification

January 26 – 27, 2015 (Mon – Tue)
San Jose, California, USA

### Wafer Fab Processing

January 26 – 29, 2015 (Mon – Thur)
San Jose, California, USA

### EOS, ESD and How to Differentiate

January 28 – 29, 2015 (Wed – Thur)
San Jose, California, USA