Issue 89 November 2016

InfoTracks

Semitracks Monthly Newsletter

Voltage Contrast Part 1

By Christopher Henderson

In this presentation, we discuss voltage contrast, one of a number of techniques that use scanning electron microscopy to aid in fault isolation. Voltage contrast can be observed as changes in the intensity of the secondary electron image.

Voltage contrast is used in four distinct ways in failure analysis. These include passive voltage contrast, biased voltage contrast, capacitive-coupled voltage contrast, and electron beam probing.

Let's first discuss passive voltage contrast. Although analysts have known about voltage contrast effects since the 1940s, the first work on passive voltage contrast was not published until 1990. Passive voltage contrast (PVC) uses the charge injection of the electron beam and the connections—or lack thereof—of features to a grounded connection on the circuit. PVC uses the electron beam to either charge a conductor positively or negatively at low accelerating voltages that are between 500 volts and 2 kilovolts. A floating conductor—such as an unconnected polysilicon gate—acquires a voltage potential similar to that of the beam. For instance, if the beam charges the gate negative, the gate appears brighter in the image because it emits more secondary electrons to achieve equilibrium. A polysilicon gate with a defect such as a short to the substrate produces a dark contrast because the conductor does not charge negatively. As a result, the conductor emits fewer secondary electrons. Passive voltage contrast is a valuable technique for locating shorted gates, single bit EEPROM floating gate failures, and open interconnect.

In this Issue:

SEMITRACKS, INC.
Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

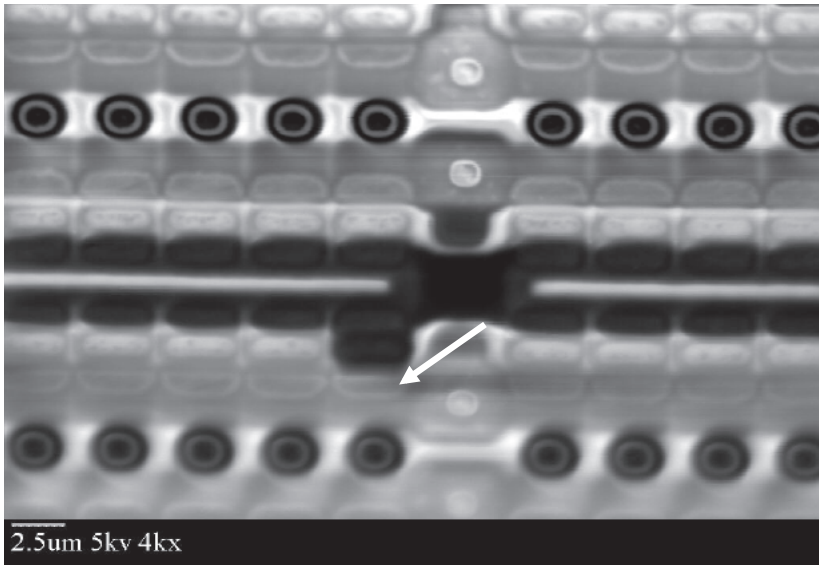


Figure 1. Image showing single bit floating gate EEPROM failure.

Figure 1 is an image generated using the passive voltage contrast technique. This image shows a small region in an electrically erasable programmable read only memory or EEPROM. The overlying metal interconnect has been removed in this sample, revealing the floating gates and contacts to the substrate. A portion of the interlevel dielectric is still intact, however. In a functional EEPROM cell, the floating gate should be electrically isolated from the rest of the circuit by either the gate oxide or the tunnel oxide, depending on the design and processing. The arrow indicates a floating gate that is shorted to the substrate. Notice that the contrast is dark. In order to obtain the image through the remaining interlevel dielectric, an accelerating voltage of 5kV was used. In order for the technique to work, the charge from the beam must penetrate to the structure of interest.

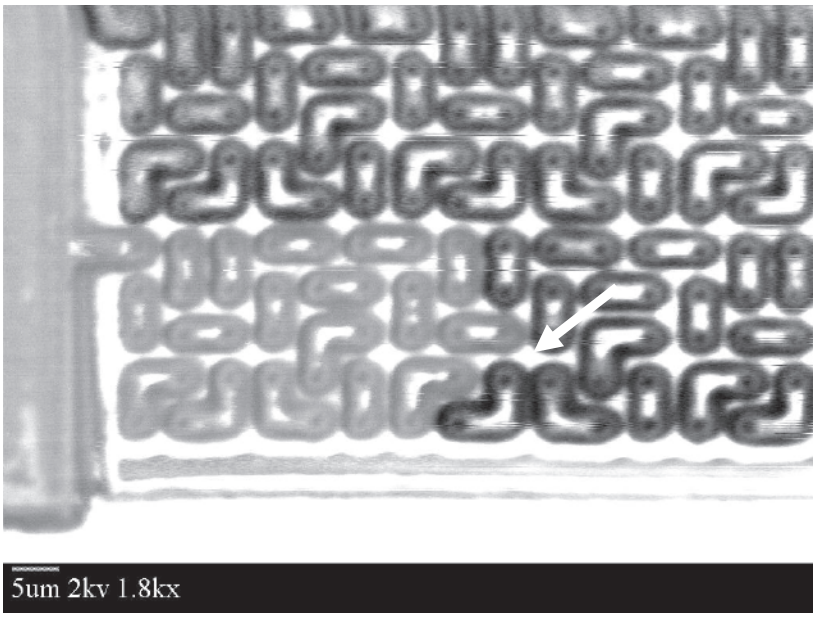


Figure 2. Open in metal daisy chain.

Figure 2 is another example of the passive voltage contrast technique. The image shows a metal contact chain with an open. The arrow indicates the location of the open, which is not directly visible through SEM inspection because the open is at the metal to silicon contact. However, the passive voltage contrast technique shows the location of the open quite nicely. One end of the daisy chain is connected to ground while the other end is not connected. This means that the portion of the chain to the lower left of the open will be floating. The electron beam will charge this portion of the chain negatively, causing it to emit more secondary electrons and appear brighter. This sample was deprocessed to expose the metal chain. The accelerating voltage used to examine this structure was 2kV.

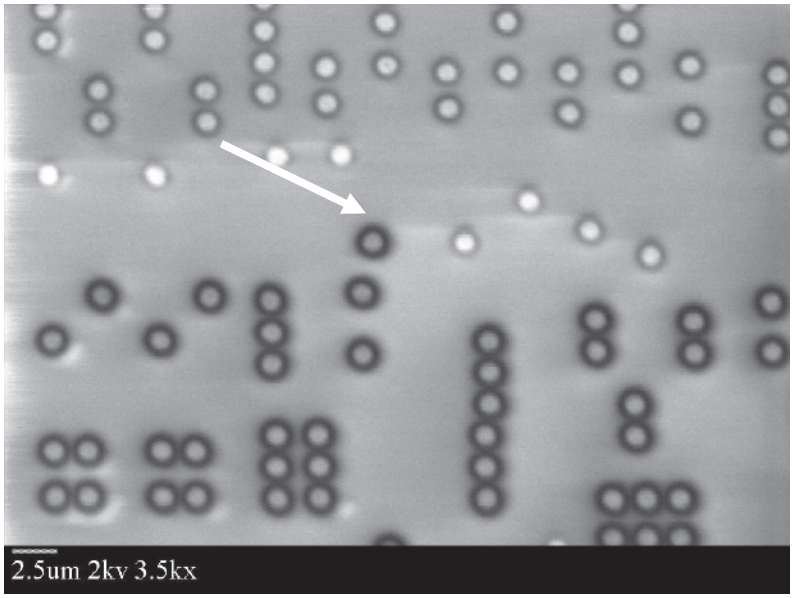


Figure 3. Shorted gate oxide.

In Figure 3 we show another example of how passive voltage contrast can be used to localize defects. The integrated circuit has been stripped to the metal-1 polysilicon interlevel dielectric. In the image, the contacts to the n-channel transistors are dark because they are tied to the substrate, which is grounded to the stage. The contacts to the p-channel transistors are bright because they are tied to the well, which is isolated from the substrate by a reverse-biased diode. The contacts to the polysilicon gate are also bright, except for the one dark contact indicated by the arrow. The gates should be bright, since they are isolated from the substrate and can charge in the presence of the electron beam. The dark gate exhibits a leakage path to the substrate.

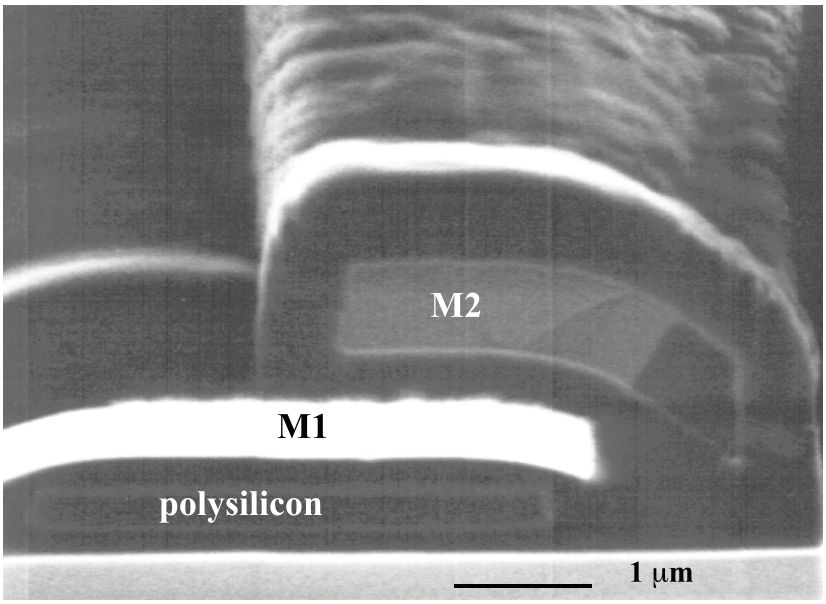
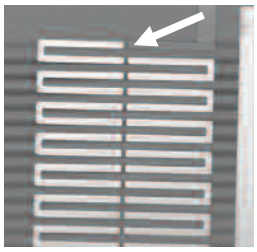
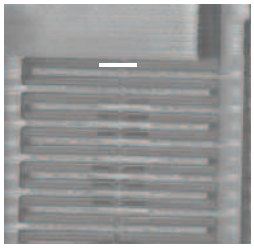


Figure 4. Passive VC effects in a Focused Ion Beam (FIB) cross section.

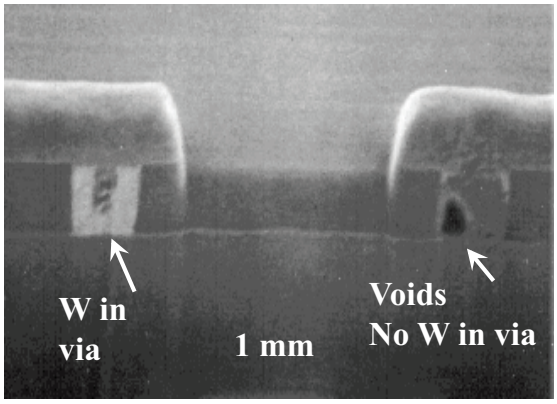
Passive voltage contrast can also be implemented and observed in a Focused Ion Beam (FIB) system. The cross-sectional image in Figure 4 shows contrast between a metal-2 line that is grounded and a metal-1 line that is floating. One can also see a grounded polysilicon line in the image.



SE Image



SI Image



FIB Cross Section
SE Image

Figure 5. PVC—defect localization on an FIB system.

In Figure 5 are several passive voltage contrast images of a test structure taken on a focused ion beam system. In the upper left, the secondary electron image clearly shows a discontinuity in the test structure. The secondary ion image in the lower left does not show this feature. Secondary ions do not exhibit the

voltage contrast effect since they are much heavier and less influenced by the charge and electric fields on the device. A cross-sectional image of the two vias in question is shown on the right. Notice that the via on the left shows good tungsten coverage, while the via on the right has no tungsten in the via.

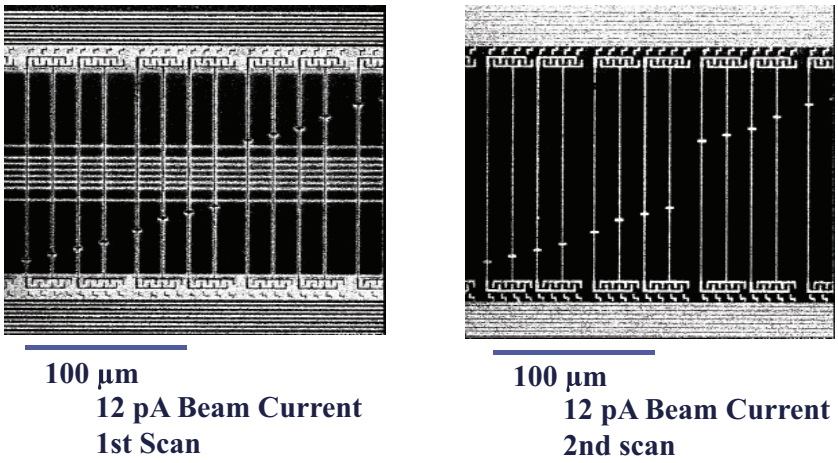


Figure 6. PVC—navigation on planarized ICs using an FIB.

Passive voltage contrast can also navigate planarized integrated circuits. The images in Figure 6 show two successive scans of the focused ion beam on a portion of a planarized circuit. As the beam scans across the device, it leaves a charge behind. The capacitance between the metal interconnect and the top surface creates an image charge that is somewhat different than the areas free of interconnect, producing contrast. The uppermost layer of metallization and the layer beneath show up clearly in the first scan on the left, while only the top layer shows up in the second scan on the right. After the beam scans the area, the effect is neutralized for the weaker capacitance between the lower metal and the surface. After several more scans, the effect for the top metal disappears as well.

Figure 7. Electron beam-based inspection and review tools.

Passive voltage contrast is now being used in yield applications. PVC is a powerful way to identify defects during the wafer fabrication process. Both KLA-Tencor and Applied Materials sell electron beam-based inspection and review tools. These tools can make use of passive voltage contrast to identify opens, shorts, contamination, and other types of defective conditions.

Although not used extensively, passive voltage contrast is nonetheless a powerful technique for isolating defects. Unlike the other voltage contrast techniques, passive voltage contrast does not require electrical connection to the pins. All you need is the ability to ground the substrate of the device to the stage. The technique can be performed in a variety of scanning electron microscopes and focused ion beam systems, as long as equipment can load a grounded sample and tilt the sample toward the secondary detector to increase the contrast. If passive voltage contrast is performed at low beam energies, the technique is non-destructive. Energies below 2kV reduce the chances of electrostatic discharge and damage from electron beam irradiation. One disadvantage to the technique is that one will likely have to remove overlying layers in a fully processed sample in order to expose the features of interest. Most of the examples shown earlier were deprocessed down to the metal layers or the gate regions of interest. Finally, passive voltage contrast requires interpretation on the part of the analyst to determine the nature of the defect. PVC does not necessarily highlight the defect itself, but rather it indicates an electrical problem on the node. Knowledge of the layout and design of the circuit can greatly aid in finding out the problem.

To be continued, next issue

Technical Tidbit

Confidence and Prediction Bands

An important aspect of statistical analysis is the confidence one has in the results. In general, the more data points one has, and the more they lie along a particular regression line, the greater the confidence one has in the results. One can visualize these graphically using confidence and prediction bands.

$$\text{Confidence} \quad X = Y \pm t_\alpha SE \sqrt{\frac{1}{n} + \frac{\left(X + X_m\right)^2}{SS_{XX}}}$$

$$\text{Prediction} \quad X = Y \pm t_\alpha SE \sqrt{1 + \frac{1}{n} + \frac{\left(X + X_m\right)^2}{SS_{XX}}}$$

The equations shown here are the equations one uses to generate confidence and prediction bands. The confidence bands are given by this equation, and the prediction bands are given by this equation, where

Y is the predicted y value

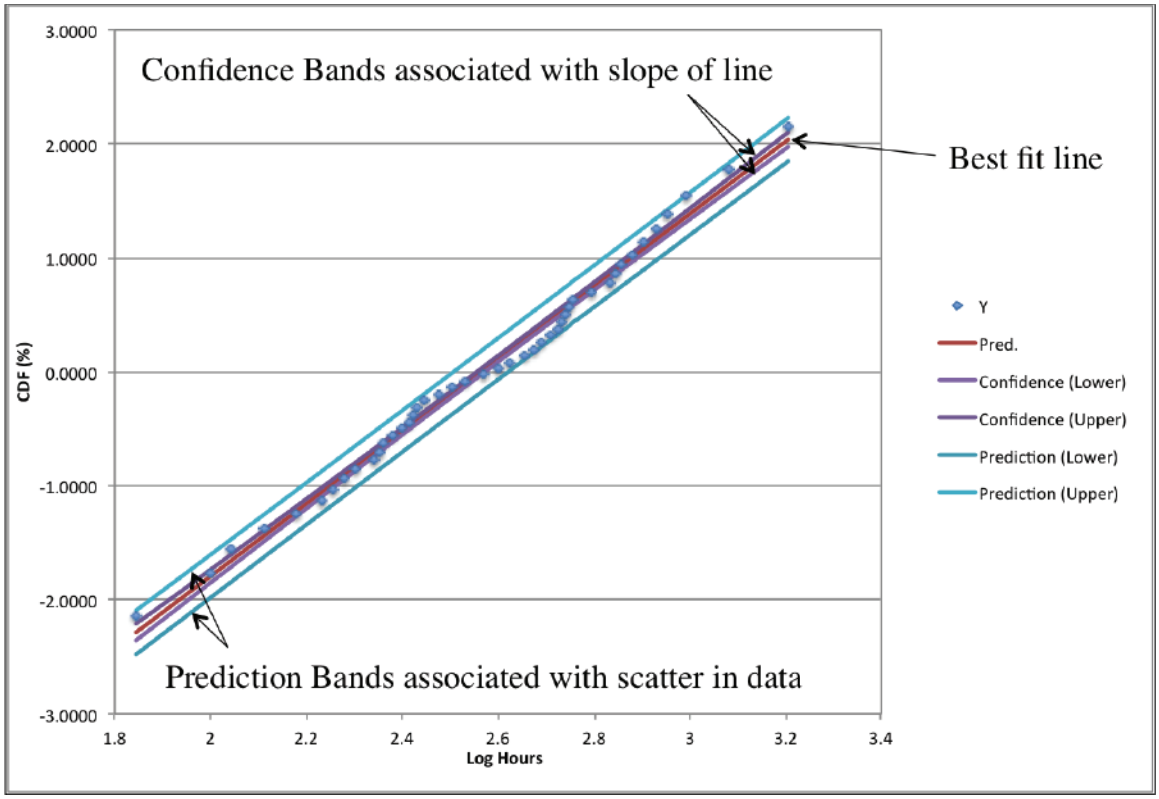
t_a is the standard deviation associated with the confidence value

n is the number of data points

X_m is the sample mean

SS_{xx} is the sum of squares of the deviation of the points from the mean

SE is the standard error, or the square root of the sum of squares divided by n minus 2.



Here we show data points plotted on a lognormal plot. We then show the prediction line in red, and the prediction bands in cyan. We also show the confidence bands for the 95% confidence level. The prediction bands form a measure of the scatter in the data. The more scatter in the data, the wider the prediction bands. The confidence bands (in purple) form a measure of the slope of the best fit line. The more the bands widen away from the T50 point, denoted as 0.0% CDF in this graph, the less confidence we have that the slope of the line is correct. Put another way, the slope of the best fit line, with 95% confidence, falls within the purple lines. This method of graphically viewing the bands can allow us to visually determine the quality of our data.

Ask the Experts

Q: In JESD47 there is a figure (Figure A) that shows a table for HTDR with cycle count (100% spec, 10% spec, and <10% spec). What does this mean?

A: There is an unofficial spec limit of 6 at% using Auger Electron Spectroscopy that has been in use since the early 1980s (J.F. Gives *et.al.,* Proc ECC 1982, pp.266) (J. Nesheim *et.al.,* ISHM 1984, pp. 70 – 78) (J. Pavio et.al., ISHM 1984, pp. 428 – 432) One can also use EDX and XPS as ways to check for fluorine, but you need to remember that the interaction volumes are different, and so the results would be different depending on the analytical tool.

Spotlight: Semiconductor Statistics

OVERVIEW

A modern semiconductor manufacturing process is one of the most difficult and complex processes to successfully control. There are thousands of variables that must all be tightly controlled in order to have a chance a repeatedly manufacturing a chip within a tight tolerance so that it can be successfully used in an electronics system. Furthermore, a modern semiconductor manufacturing process generates an incredible volume of data. This requires that engineers be able to not only choose the right data to examine, but also examine it in such a way as to understand the behavior of the process. We do this through statistical process control. This course is designed specifically for engineers who work in semiconductor manufacturing operations. We provide numerous real-world examples from semiconductor operations such as wafer fabrication, assembly, test, and reliability.

WHAT WILL I LEARN BY TAKING THIS CLASS

By focusing on tried and true methods for SPC, participants will learn the appropriate methodology to successfully identify problems, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into four segments:

1. **SPC Foundational Elements.** Participants learn about the foundational elements of statistical process control, including: basic statistics, methods to visualize data, process capability, and basic problem solving.
2. **Process Monitoring Techniques.** Participants learn the various techniques for monitor a semiconductor process. They discuss on-wafer measurements like thin film measurements, defects, and electrical measurements.
3. **Process Control.** Participants learn about the various control charts and how to identify key variables in process control charts. They also discuss the fundamentals of process control and the various control methods.
4. **Design of Experiments.** Participants learn about Analysis of Variance (ANOVA) and other DOE methods like Factorial and Taguchi methods.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and methods used in SPC.
2. Participants will be able to identify the different methods to visualize data related to SPC.
3. The seminar will identify the advantages and disadvantages of the various control charts that are used for SPC.
4. The seminar offers a variety of example problems, so the engineer can gain an understanding of the types of issues they might expect to see in their job assignment.
5. Participants will be able to set up a design of experiments to gather more data related to a particular problem.
6. Participants will understand the types of data on might gather, related to SPC.
7. Participants will be able to set up a control chart and monitor it for excursions and analyze the results.

COURSE OUTLINE

Day 1 (Lecture and Lab Time 8 hours)

1. Wafer Fab Related SPC
    a. Statistical Process Control
        i. Control Chart Basics
        ii. Control Charts for Variables
        iii. Moving Average Charts
        iv. X and R, S
        v. How to Monitor a Control Chart
        vi. Multiple Equipment same process control charts
        vii. Multivariate Control
        viii. Distributions
        ix. Cusum Charts
    b. Process control index Cpk and Ppk
    c. Defect Density & Yields
    d. Wafer Acceptance Test parameters
        i. Sort yield & Defect Density
        ii. Set outlier limit
        iii. Statistical Bin Limits methodology
    e. Design of Experiments
        i. Randomized Block Experiments
        ii. Two Way Designs
        iii. Student T-test
        iv. Analysis of Variance (ANOVA)
        v. ANOVA Table
        vi. Taguchi Methods
2. Assembly and Packaging Related SPC
    a. Variables
    b. Control Charts for Variables
    c. Process Capability Index (Cpk) - Review
    d. Multiple Equipment
    e. DOE Bonding optimization

Day 2 (Lecture and Lab Time 8 hours)

1. Test Related SPC
    a. Gauge Repeatability & Reproducibility Principles
    b. Test Limits
    c. SBL Setting
    d. Tester correlations
    e. Average Outgoing Quality
    f. Sample Size, AOQ, LTPD, etc.
    g. Confidence interval
    h. Exercises with Marvell-supplied data

2. System Level Test Related SPC
   a. Reliability Statistics
   b. Distributions
      i. Normal Distributions
      ii. Lognormal Distributions
      iii. Weibull Distributions
      iv. Exponential Distribution
   c. Gathering Accelerated Testing Data
   d. PPM and FITS Calculation
   e. Exercises with Marvell-supplied data
3. Reliability Statistics
   a. Gathering Accelerated Testing Data
   b. In-class Exercise: Determining Time to Failure
   c. Using the Poisson Distribution to Estimate PPM, FITS
   d. In-class Exercise: PPM and FITS Calculation
4. Field Returns and SPC
5. Wrap-Up Discussion

IRPS

International Reliability Physics Symposium

2017 IEEE International Reliability Physics Symposium

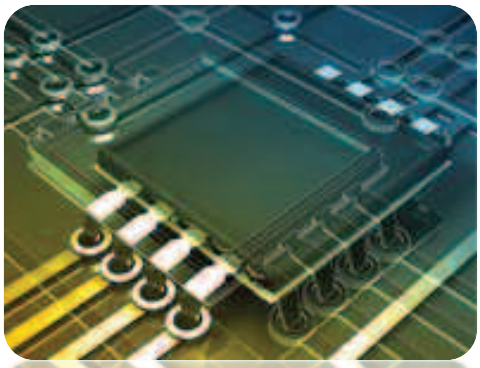
IEEE

April 2-6, 2017
Hyatt Regency Montery Hotel and Spa
1 Old Golf Course Road
Monterey, CA, USA 93940

Registration is available at www.irps.org

Chris Henderson, IRPS Board

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com during the symposium!



Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
Jan 30 – Feb 2, 2017 (Mon – Thur)
Portland, Oregon, USA

Advanced CMOS/FinFET Fabrication
Feb 6, 2017 (Mon)
Portland, Oregon, USA

Semiconductor Statistics
Feb 7 – 8, 2017 (Tue – Wed)
Portland, Oregon, USA

Semiconductor Reliability
Mar 13 – 15, 2017 (Mon – Thur)
Singapore/Malaysia

Defect Based Testing
May 3 – 4, 2017 (Wed – Thur)
Munich, Germany

Failure and Yield Analysis
May 8 – 11, 2017 (Mon – Thur)
Munich, Germany

Semiconductor Reliability and Qualification
May 15 – 18, 2017 (Mon – Thur)
Munich, Germany

Semiconductor Statistics
May 22 – 23, 2017 (Mon – Tue)
Munich, Germany

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).
To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

~

For more information on Semitracks online training or public courses, visit our web site!
http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!