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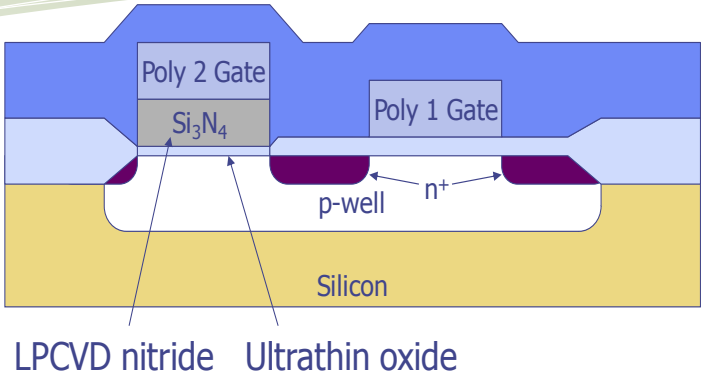

An SNOS two-transistor memory cell

[inside this issue]

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A Brief History of Non-Volatile Memory

[By Chris Henderson]

Part Two

Non-volatile memory technology, which can hold data with the power removed, has become critical to devices such as PDAs, cell phones, and digital cameras. In the last issue of InfoTracks*, we presented the background of one of the original non-volatile memory technologies, the metal nitride oxide silicon (MNOS) technology. Part Two of this informative three-part series will cover an improvement over MNOS called silicon oxide nitride oxide silicon (SONOS) technology, and its predecessor, silicon nitride oxide silicon (SNOS). Next, we'll discuss the floating gate avalanche injection MOS or FAMOS transistor, used extensively in ultraviolet erasable memory.*

While attempting to improve MNOS performance during the 1970s, Takaaki Hagiwara and his colleagues at Hitachi developed the SNOS. They determined that coupling a low pressure chemical vapor deposition silicon nitride with a high-temperature hydrogen anneal of the nitride-ultrathin oxide-silicon interface increased memory retention times to over 10 years. To make the power supply voltage in the read mode compatible with other contemporary standard logic components, Hagiwara et al. reduced the voltage to five volts. They were also able to reduce access times to fewer than 150 nanoseconds—more than six times faster than contemporary MNOS memories. Since performing a high temperature anneal requires temperatures in excess of the aluminum melting point, the technique cannot be performed on memories that utilize aluminum gate technology.

The diagram above depicts the SNOS two-transistor memory cell. The SNOS memory cell permits full byte programming. The gate on the left is the SNOS transistor, while the gate on the right is the select transistor for the memory cell. The ultrathin oxide measures approximately 10 to 20 angstroms and the low pressure CVD silicon nitride measures about 500 angstroms.

The SNOS process requires two polysilicon deposition steps. The first deposition step, poly one, forms the access transistor gates and the rest of the logic gates on the circuit. The second step, poly two, forms the control gate for the SNOS transistor.

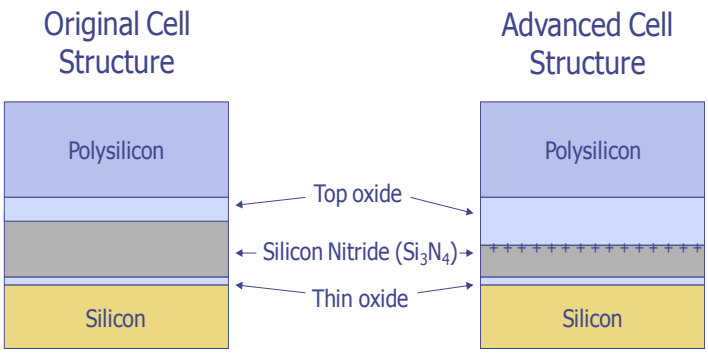
Although SNOS devices possess a more efficient write time than MNOS memories, SNOS technology still has limitations. One particular problem is hole injection from the gate. Especially when the nitride is thin, hole

injection from the gate can limit the charge retention capabilities of the cell. The limitations of SNOS memory fueled scientists' desire to create a more efficient and reliable cell.

To address the limitations of SNOS memory, Peter Chen and others at NCR developed the silicon-oxide-nitride-oxide-silicon (SONOS) memory cell. After the memory cell's initial development in the mid 1970s, researchers fabricated SONOS devices with a steam oxidation of the nitride film. However, Chen et al. discovered that oxide deposition was also possible. Using the SONOS technology discovered by Chen, several manufacturers, including Seeq Technology (later acquired by LSI Logic) and Northrop Grumman, introduced commercial memories. Today, Freescale Semiconductor (formerly Motorola), Philips, and other companies continue to investigate SONOS for embedded memory applications in logic devices.

The diagram on this page demonstrates the basic cell structure for the SONOS transistor. As with the SNOS memory cell, a thin oxide is grown on the silicon and a low pressure CVD nitride deposition is performed. Then, the structure is annealed to improve its thin oxide properties. The top oxide can be grown using a steam oxidation at temperature of around 975°C or using a CVD process. The oxide layer serves as a barrier to prevent charge from entering or leaving the storage cell. Since the barrier is now larger, the top oxide reduces the possibility of hole injection from the gate. In Chen's original structure, the thin oxide measured approximately 20Å, the nitride measured approximately 400Å, and the top oxide measured approximately 150Å.

While the original concept for SONOS enhanced retention and improved on SNOS memories, the continued scaling of integrated circuits reduced retention times. Thinning the nitride caused damage to the cell over an extended period. Because the top oxide, an oxynitride, did not have the superior dielectric



Basic cell structure for an SONOS transistor

qualities of the thin oxide, holes became trapped close to the gate electrode and tunneled through the top oxide. As the electrons tunneling through the oxide broke the bonds in the silicon dioxide molecule, the cell gradually accumulated damage. Also, the electric field present during tunneling could break the bonds, damaging the oxide. Thus, researchers attempted to reduce tunneling by increasing the thickness of the top oxide or switching to a deposited oxide.

In the late 1960s, Khang and Sze at Bell Laboratories first proposed the Floating Gate Avalanche Injection MOS (FAMOS) memory cell. While at Intel in the early 1970s, Dov Frohman-Bentchkowsky developed working memories based on the FAMOS concept. In a FAMOS cell, a source or drain injects charge into the floating gate region. The operation of the cell relies on tunneling current, so the thickness of the oxide between the floating gate and the channel controls the write times. Early devices contained rather thick oxides, so the write times were relatively slow.

The FAMOS technology was easier to process, and scaled to smaller feature sizes more readily. Ultimately, FAMOS technology replaced SNOS and SONOS devices, as it permitted faster write times and better control over the write voltages. FAMOS technology forms the foundation of modern NOR flash memories, which will be covered in Part Three next month.

Technical Tidbit

[The Half Adder Function]

The half adder, a combinational logic function that adds two bits, is a common building block in digital circuits. Half adders are used to construct a variety of functions such as full adders of various sizes and multipliers. Adding a carry signal to a half adder yields a full adder. The truth table, shown in Figure 1, gives all combinations of the inputs and the resulting outputs. X and Y are the two inputs, C is the carry output, and S is the sum output. Because the truth table adds X and Y in binary, 0 plus 0 is 0, 0 plus 1 is 1, 1 plus 0 is 1, and 1 plus 1 is 0 with a carry of 1.

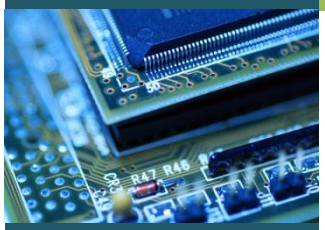
The figure on the next page illustrates four possible implementations of the half adder and full adder functions. The equation below each set of gates shows the corresponding logical functions. Recall that the AND gate equals the dot in the logical equation and the OR gate equals the plus sign. The lower right implementation uses an exclusive OR gate, represented by the circled "plus" sign. Many IC designers implement the half adder or full adder as a standard cell in the digital logic library for the chip design.

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$S = x'y+xy'$

$C = xy$

The truth table



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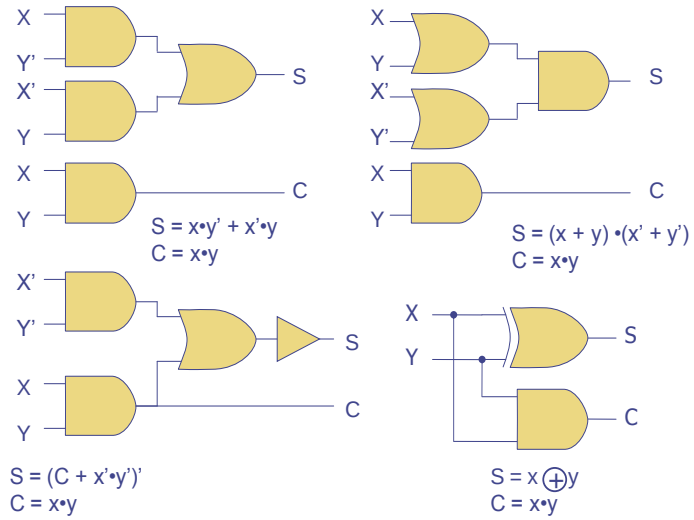

Technical Tidbit: Four possible implementations of half adder and full adder functions.

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Questions & Answers

Q: Is there a specification for overdrive on probe cards?

A: There is not a specification per se, but there are best practices. The best practice on pads in the 80-100 micron size use 75 microns of overdrive. For pads in the 30-50 micron range, an overdrive of 35-50 microns is more appropriate. Overdrive refers to overdrive in the z-axis.

To post, read, or answer a question, visit http://forums.semitracks.com/.
We look forward to hearing from you!

Course Spotlight

[CDMA & EV-DO Technology]

Code Division Multiple Access (CDMA) is an increasingly popular method for handling higher volumes of calls. This spread spectrum technique is resistant to inference and jamming, provides for more calls to be made on a single frequency, allows for frequency reuse, and permits soft handoffs. Evolution Data Optimized, or Evolution Data Only (EV-DO), is designed as an evolution of the CDMA 2000 standard that supports higher bandwidths, enabling a wider range of wireless data services.

To correctly and efficiently implement both CDMA and EV-DO standards, engineers must possess in-depth knowledge of the technology, standard, algorithms, and issues associated with the two wireless standards. We designed our ***CDMA and EVDO Technology*** course to emphasize these essentials and delve into current issues related to manufacturing next-generation devices. This course is appropriate for engineers, technicians, and equipment manufacturers designing 1xEV-DO products and network operators building and optimizing 1xEV-DO networks.

The course will cover the following areas:

- How to apply CDMA and EV-DO technology in today's high volume wireless data applications
- The IS-856 core EV-DO standard and the IS-871 interworking standard
- The objectives, philosophy, and steps involved in optimizing the over-the-air performance of 1xEV-DO networks.
- How to construct and evaluate CDMA and EV-DO wireless networks.
- And more!

Semitracks' CDMA and EV-DO Technology course combines lectures, hands-on classroom exercises, experiments using CDMA equipment, and question/answer sessions to help you gain concrete, applicable skills. The course will offer not only practical experience, but also additional pages of reference material as an invaluable on-the-job resource.

Click here for more information and a course outline. For more information on the other courses we offer, visit www.semitracks.com.