Issue 16 October 2010

InfoTracks

Semitracks Monthly Newsletter

Visit Semitracks at ISTFA

The International Symposium for Test and Failure Analysis (ISTFA) will be held November 14-18 at the Intercontinental Hotel in Dallas Texas. Semitracks will be exhibiting at the conference, please stop by and see us at booth 217.

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Training: The Need is Becoming Critical – Part 1

By Christopher Henderson

Introduction

The design, fabrication, reliability, and analysis of semiconductor components has become an increasingly complex task. Today's engineer is called on to pull "a rabbit out of a hat." Every year, the feature sizes get smaller, the designs get bigger, and the customer wants it made faster. With this in mind, how should we train our engineers to perform this daunting task? There are several major thrusts our education/training efforts need to take if we are to be successful developing and fielding modern semiconductor components. These thrusts include: process, technology, cross-training, and techniques. For the purposes of this paper, I will discuss the history of training activities in the failure/product analysis discipline, and describe where this area is heading. Training for design, packaging, processing, reliability, and test, although different in content, is similar in scope, since today's semiconductor scientists, engineers and technicians must increasingly know more about the overall process in order to succeed in their areas of expertise.

Historical Perspective

In 1966, Fairchild Semiconductor introduced the quad, two-input NAND gate (see Fig. 1). Soon afterwards, Texas Instruments, Motorola, National Semiconductor and others introduced their own lines of standard logic parts. In the late 1960's much of the integrated circuit development was performed for the U.S. military. At this time, the military also began a push to increase the

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Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

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reliability of its systems. This brought about the need for analysis capabilities to understand failure mechanisms associated with these integrated circuits. As these parts grew in popularity, the requirement for failure analysis grew. During the late 1960's many companies began taking the first steps toward establishing what we now know as a failure analysis laboratory. The failure analyst was born.

In the late 1960's, much of the failure analysis work was done on field returns. Systems companies returned devices that failed to the manufacturer for analysis. This meant that the analyst served in a reactive mode to problems the customer might experience. The semiconductor manufacturers produced components in relatively low volumes; they also manufactured the same components over a long period of time. This meant that the analyst could feed back information from field returns to the manufacturing line in time to make an impact. The process engineers could then make changes to the manufacturing line that would correct the problems seen by the customer.

In the late 1960's, product engineers performed failure analysis for the most part. The product engineer knew everything there was to know about their product. For example, a competent product engineer knew the schematic, recognized the layout, could map between the schematic and layout, knew the processing steps, understood the mask levels, knew how to test the part, knew the packaging process, and understood the customer's requirements (from regular visits and/or telephone conversations).

Quite often, failure analysis could be accomplished with a curve tracer, some package decapsulation tools and techniques, and an optical microscope. More subtle problems required a scanning electron microscope (SEM) and possibly energy dispersive spectroscopy (EDS). The investment in failure analysis tools was modest. $250,000 bought all of the tools that were necessary to do most any analysis job. More importantly, the investment in skills and training was modest. A competent electronics technician could perform and manage all aspects of the analysis.

In the late 1960's there was no training program for analysts. Public training courses, like those offered by Bud Trapp, John Devaney, and Howard Dicken, were still a decade away. Training occurred "on the job." The analyst talked to the process engineers to understand the process, the designers to understand the layout, schematic, and test procedures, and the packaging engineer to understand the packaging process. The rest of his or her training came from experience. Good analysts were typically individuals who had years of experience and kept good records that allowed them to look for trends and recurring problems.

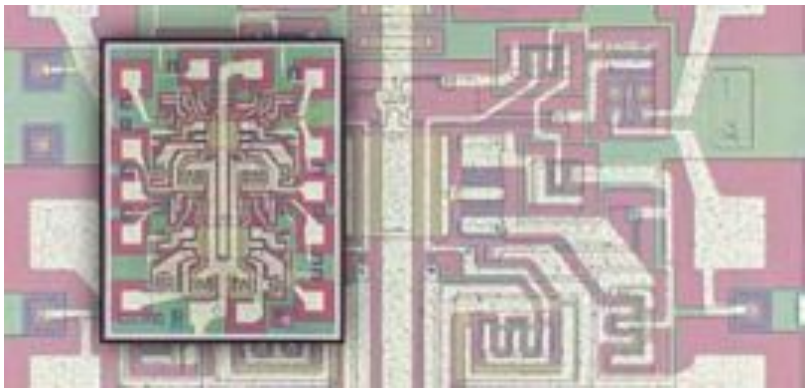


Fig. 1. Photograph showing the Fairchild Semiconductor quad, two-input NAND integrated circuit (photo courtesy Fairchild Semiconductor).

Ask the Experts

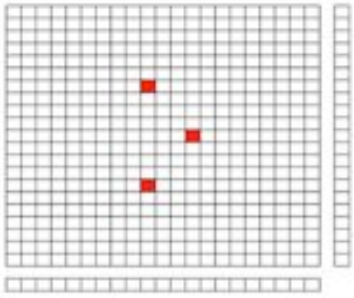
Q: I have a question regarding package decap and copper wires. I am experiencing problems keeping the copper wires from being attacked while etching open the packages.

A: Packages with copper wires can be quite difficult. The success of opening a package with copper wires is directly related to the type of encapsulant used and the gauge and density of copper wires used in the package itself. The more dense the wires, the more difficult the application. For example, LSI Logic created a package that had 3 rows of bonds in a BGA. It is almost impossible to clear all of the encapsulant material from between the copper wires and expose the bonds without some damage to the wires. The best way to approach packages with either unpassivated copper on the surface of the die or copper wires is to start with a 3:1 mix of 90% fuming nitric acid and 20% fuming sulfuric acid at 37-40 degrees Celsius. The etch will be longer, but the chance of copper preservation is far better.

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Technical Tidbit

Built-in Self Repair



A memory array with several failing bits.

Memory elements now comprise most digital logic devices and Systems on a Chip (SoC). Because memory is densely laid out, it is often most susceptible to failure. Today, some memories include the ability to repair themselves. Self-repair is normally accomplished with redundant rows and columns. In order for this to work, one must be able to identify the fault, determine whether it is an aggressor or victim cell, and switch in the other elements through fuses, flash memory, or some other form of permanent storage. Some of these problems can be identified with built-in self test (BIST). For new failure modes and defects, the BIST algorithm must be updated. Therefore, there is a requirement for the ability to program the BIST engine for updates.

The image on the right shows an example of a memory array with several failing bits. If one bit fails, the solution is straightforward: replace it with a new column or row. If more bits are failing, then you need to evaluate the failure locations with optimal repair

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Announcements: ISTFA 2010

November 14-18, 2010
InterContinental Hotel
Dallas, TX, USA

Stop by and see us at booth 217

Enrich your career at the 36th International Symposium for Testing and Failure Analysis, November 14-18 in Dallas, Texas. Acquire the latest knowledge from the field's leading professionals with six days of tutorials, short courses, technical presentations, panels, and user groups. Research leading edge instruments and solutions at the industry's largest dedicated equipment expo. Meet and network with hundreds of your peers from novice to expert. Find out more about ISTFA 2010.

Course Spotlight: Semiconductor Reliability

A semiconductor device is only as good as its reliability: the probability that it will perform its function under specified conditions for a set time. Semitracks' 3-day Semiconductor Reliability training course offers detailed instruction on how to determine what failure mechanisms might occur, test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions, and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur at both the die and package levels. These include time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, etc.
3. **Test Structures.** Participants learn how test structures can be designed to test for a particular failure mechanism.
4. **Test Strategies.** Participants learn the basics of testing test structures, conducting design screening tests, and performing burn-in testing effectively. Learn more.

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solutions. Built-In Redundancy Analysis (BIRA) or offline analysis is usually necessary to resolve multiple failing bits.

There are several repair solutions for memory defects. The first, laser repair, is a time-consuming operation that requires three steps at wafer probe to implement. Another is E-fuse, a high current solution that fuses interconnect to re-wire a circuit. The technology was developed by IBM and uses a reliability failure mechanism called electromigration for creating the open connection. Still another repair solution is the use of flash memory. Flash memory can be re-written to alter the logic on an IC. However, the technology requires special wafer processing steps and the use of high voltage. Finally, soft repair is an option. In the soft repair solution, the chip evaluates a repair solution each time it powers up. It is a room temperature test, but can detect new defects as the chip ages. It requires a longer boot sequence though, so it may not be useful in certain applications.

At the system design level or the chip development level, you might ask if a chip should have memory repair. The answer depends on the application, which is driven by cost and probability of failure. The cost of a chip increases when the extra repair circuitry is added to the memory. Extra cost is also associated with additional test time to repair and retest, since these actions must occur on the tester. The probability of failure is also a key issue since the consequence of failure may differ from application to application. Factors involved include the percentage of the die with memory, the probability of failure of the device, the probability of a successful repair, and the memory optimization for successful repair.

Upcoming Courses

ESD Design and Technology
November 9-11, 2010
Austin, TX, USA

ESD Design and Technology
December 14-16, 2010
Kuala Lumpur, Malaysia

Failure and Yield Analysis
January 18-21, 2011
Kuala Lumpur, Malaysia

IC Packaging Metallurgy
January 24-25, 2011
San Jose, CA, USA

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or e-mail us at info@semitracks.com.

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by email at jeremy.henderson@semitracks.com.

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our website!

http://www.semitracks.com