

# InfoTracks

Semitracks Monthly Newsletter

## New Semitracks Blog!

In order to keep our readers better up-to-date and informed, Semitracks Inc. has launched its new blog!

Read more, Page 3

### Source and Drain Extensions Part II

By Christopher Henderson

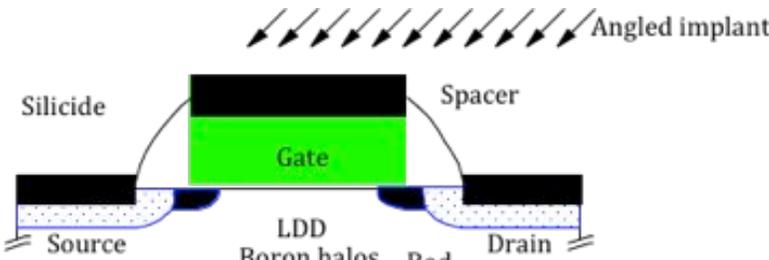


Fig. 2. Diagram showing angled implant concept.

Let's examine short-channel transistors and halo optimization more closely. In advanced technologies, we want to minimize the diffusion of the dopant atoms. This is especially important with the halo profile. One can improve the halo profile with a flash anneal. This is also important in mixed-signal, digital and RF analog applications. If the halo reaches to the surface, it can alter the effective channel length of the transistor, creating an effect like the reverse short channel effect. As the drain voltage increases, the depletion will spread beyond the surface halo, decreasing the threshold voltage and increasing the saturation drain current. This is similar to a short channel effect, but is instead observed in long channel transistors and degrades the early voltage.

Another technique used in the lateral asymmetrical channel. This technique, where dopant atoms are implanted at just one fixed angle to form a single halo or pocket, increases the contribution associated with velocity overshoot because of the built-in field at the source end of the transistor. It does improve analog parameters though.

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**SEMITRACKS, INC.**

Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

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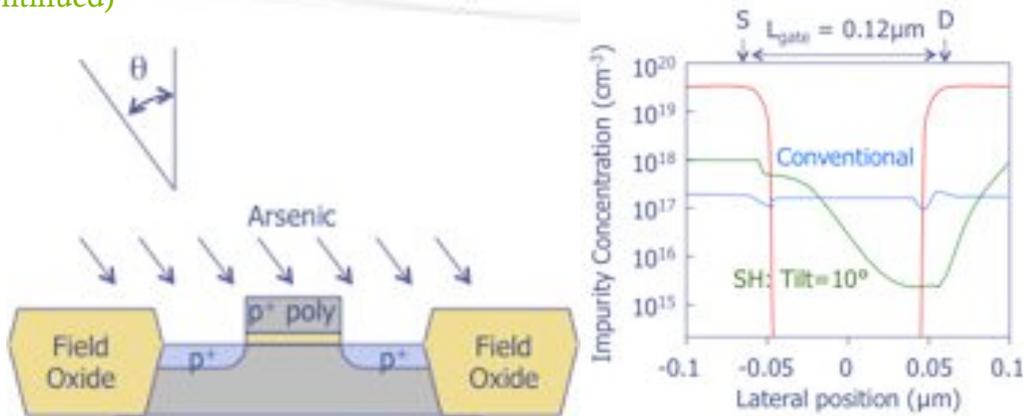


Fig. 3. Diagram showing lateral asymmetrical channel concept and implant profile.

Let's move on and discuss raised source/drain regions. This technology involves implanting lightly-doped drain regions or extensions to form spacers. The raised portion of the structure is created through selective epitaxial growth on the junction region. One then implants a dopant into this structure and drives it in using rapid thermal anneal. This diagram doesn't show the silicide layer. This approach drives up the cost of the technology through extra steps, and it is not clear how well this will work for future transistor technologies. However, there are some significant advantages. The implant damage is confined to the epitaxial layer, and it eliminates transient-enhanced diffusion. The junction is formed by driving in the dopants from an elevated location, which helps prevent overdriving. There is also sacrificial silicon for the silicide reaction. It forms a borderless contact, and it reduces the contact aspect ratio.

**Stay tuned for the conclusion of this article in November!**



# ISTFA/2011<sup>®</sup>

**November 15-16, 2011**

**San Jose, California**

Semitracks will be demonstrating its Online Training System this year at ISTFA. Stop by and see us at Booth #327.

Learn more about this conference at:

<http://www.asminternational.org/content/Events/istfa/>



## Ask the Experts

**Q: Is oxidation-enhanced diffusion prominent or negligible?**

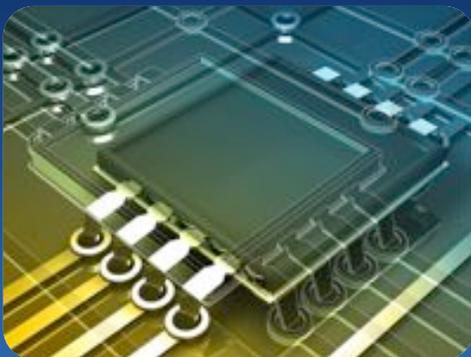
**A:** The answer depends on the dopant elements involved. Oxidation generates excess silicon self-interstitials, which enhance the diffusivities of atoms that diffuse with a significant interstitialcy component. This includes Boron, Phosphorus, and Arsenic. It retards Antimony, which diffuses primarily by the vacancy mechanism.

*To post, read, or answer a question, [visit our forums](#).  
We look forward to hearing from you!*

## Technical Tidbit: High Aspect Ratio Issues

In this technical tidbit we'll discuss some issues and approaches to dealing with high aspect ratio structures like contacts and vias. A problem related to etch is the subsequent deposition step. Deposition is especially challenging with high aspect ratio structures. \*Conventional Physical Vapor Deposition exhibits problems such as overhang at the top, or re-entrant top corners, thinning on the floor and lower sidewalls, discontinuities at the floor to sidewall corner. As such PVD can no longer meet specifications for many IC structures. \*An improvement on PVD is physically collimated PVD confines the deposition angle to near zero, which improves film conformality at the floor of the structure, but it limits through-put. It is also not appropriate for ultra-thin films.

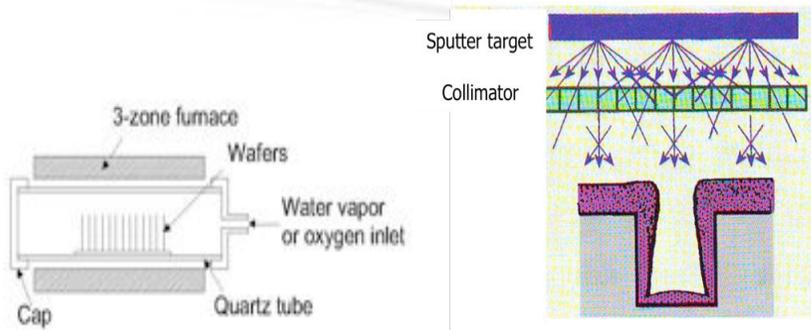
## New Semitracks Blog!



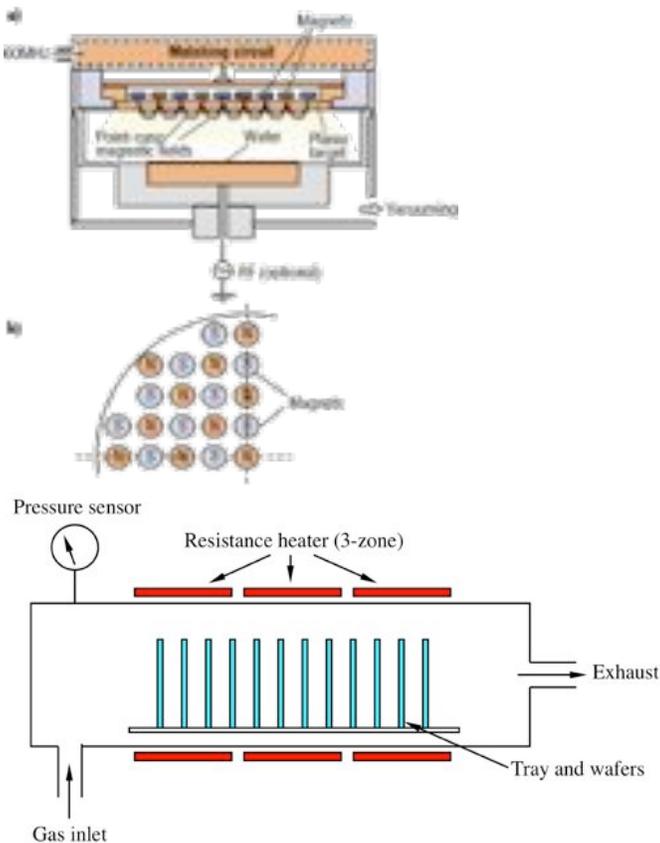
Semitracks has started a blog to keep you up to date on industry developments and items that affect Semiconductor Product Engineering and Reliability. In addition to industry developments, we'll include some short articles on technology items of interest. These may vary from historical items that help place current developments in context, to future developments that are likely to affect the industry. If you have comments or feedback, or topics you would like to see addressed, please feel free to e-mail us at [info@semitracks.com](mailto:info@semitracks.com).

See it for yourself at:

<http://www.semitracks.com/index.php/en/blog>



Yet another approach to PVD is ionized PVD with re-sputter. In this approach one replaces conventional PVD for metal deposition on ICs. The metal atoms are ionized in a plasma and accelerated to surface, producing a directionality. This improves floor coverage, gives a smooth morphology, and results in high-purity films. The added energy can be adjusted to be high enough to re-sputter metal from the floor onto the sidewalls. This yields improved step coverage but can lead to difficulty at the lower corners of a trench. In some of today's ICs, the aspect ratio exceeds the range of ionized PVD conformality. \*As a result, many deposition steps are done using Chemical-Vapor Deposition, or CVD. With CVD, one can achieve uniform deposition on all surfaces. However, it can be difficult to control ultra-thin films.



Technical Tidbits



## Upcoming Courses

[Semiconductor Reliability](#)

January 16-18, 2012 - San Jose

[Wafer Fab Processing](#)

January 16-19, 2012 – San Jose

[Polymers in Electronics/FTIR](#)

January 17-18, 2012 - Phoenix

[Failure and Yield Analysis](#)

January 23-26, 2012 – Cambridge, UK

[Defect Based Testing](#)

January 30-31, 2012 – Cambridge, UK

## Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or e-mail us at [info@semitracks.com](mailto:info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by email at [jeremy.henderson@semitracks.com](mailto:jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

For more information on Semitracks online training or public courses, visit our website!

<http://www.semitracks.com>

To post, read, or answer a question, [visit our forums](#).  
We look forward to hearing from you!