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Substrate Materials III

By Christopher Henderson

Some companies are beginning to use silicon as an interposer or substrate technology. Silicon has key advantages. One, it is matched to the die in terms of the coefficient of thermal expansion. Two, one can use standard wafer lithography and processing techniques on the interposer. This allows one to use fine geometries. However, the use of a silicon interposer requires a method to connect signals from the front side of the interposer to the backside. This means the use of through silicon vias, or TSVs. The TSV is maturing—but is still a technology that is quite new and untested—so many manufacturers are wary of their use in high reliability applications. This is an example of the Xilinx 2.5D FPGA package structure in cross section. Xilinx uses a silicon interposer with through silicon vias to route signals from one FPGA slice to the other. Notice that they still use a laminate substrate to form the BGA package.

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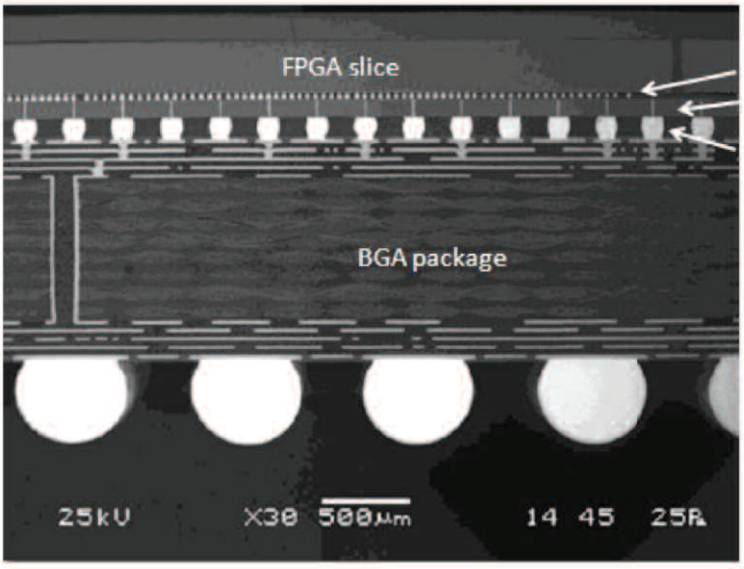
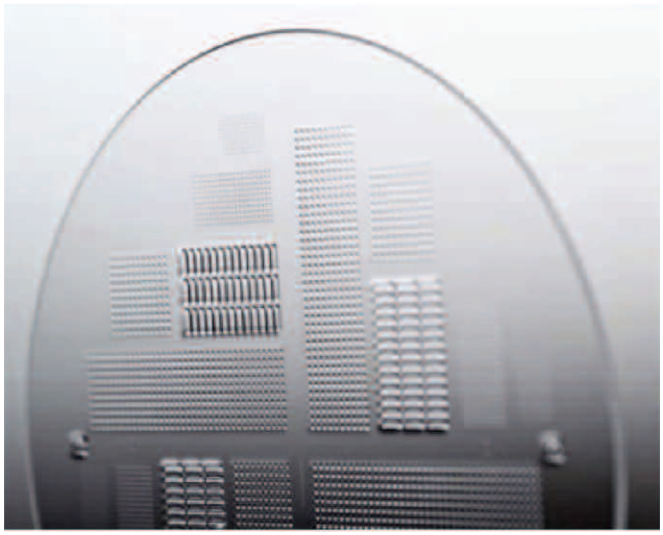
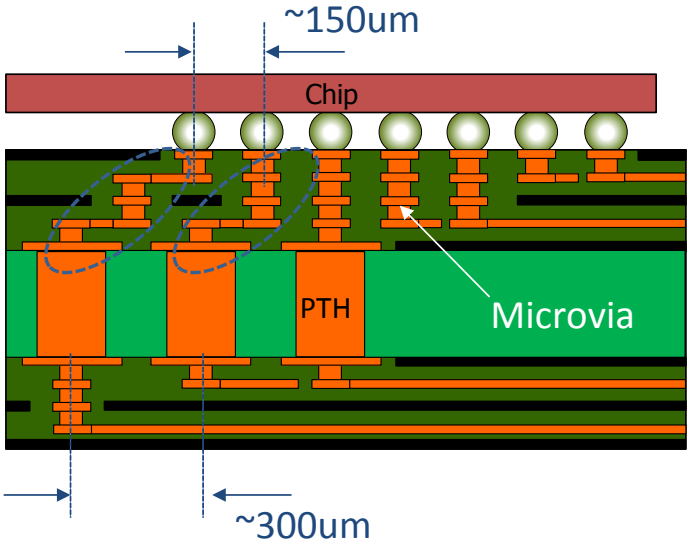


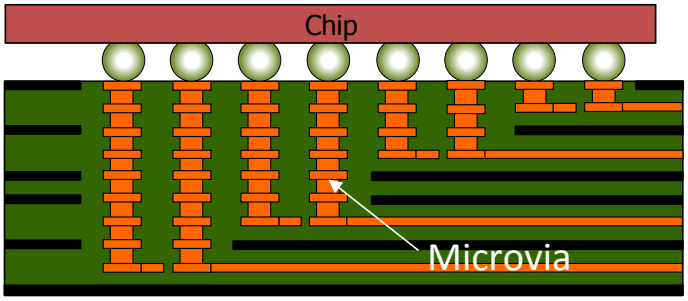
Another substrate material under investigation is silicon dioxide, or glass. The main advantage for glass is that—in addition to the fact that there is a good CTE match to the chip—the dielectric constant is much lower than that of silicon. Silicon dioxide is 3.9, whereas silicon is 11.7. However, glass is not an easy material with which to work. Scientists have demonstrated through glass vias, but haven't demonstrated manufacturing consistency and high reliability yet. As this technology evolves, this may become a worthwhile alternative to silicon interposers.

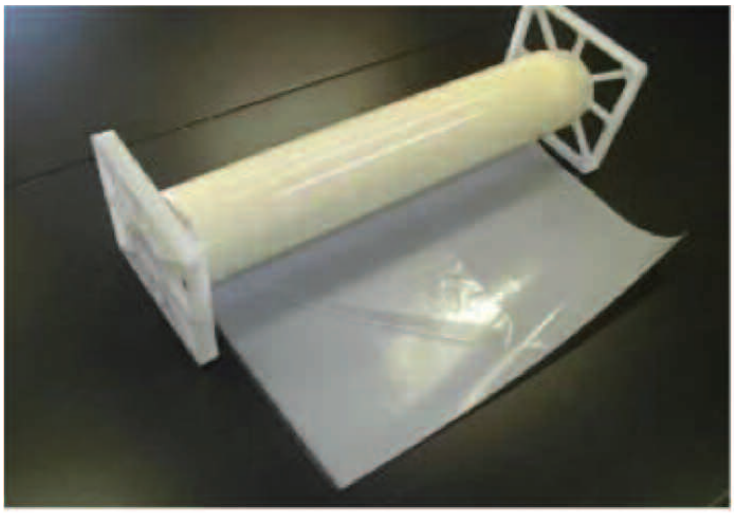


Another option engineers are exploring is coreless substrates. In a standard build-up package, there is a core material made from FR4 or BT epoxy laminate as we discussed earlier. A build-up package requires a fan-out region to match the bump and/or the line pitch to the plated through hole pitch. We highlight this region with the yellow ellipses. In a coreless package there is no core material, just build-up materials. This facilitates direct signaling. Designers can use all of the layers for signals, and the approach maximizes wiring efficiency. It also reduces impedance mismatches that occur as the result of the plated-through holes. Co-planarity is also better with a coreless package. The major issue with coreless substrates is warpage. Warpage is up to four times worse with a coreless substrate due to the lack of a

rigid core to hold everything in place. As a result, not many manufacturers are using coreless substrates. However, Sony uses this technology in the latest version of their Cell processor family.







Cover film (OPP 16um)
Resin layer (10-100um)
Support film (PET 38um)

The major player for coreless package build-up materials is Ajinomoto. The Ajinomoto Build-up Film—or ABF—is used extensively in the industry already on substrates with cores, and now used for coreless build-up as well. ABF is a three-layer polymer system, with a polyethylene terephthalate (PET) support film, a resin layer, and a cover film. One can deposit copper on the thin to create interconnect traces. Ajinomoto has evolved its ABF to remove the halogens, lower the coefficient of thermal expansion, and allow for narrower vias. It is used widely as a standard build-up material, and is now in limited use for coreless substrates.

This table shows the common materials properties for substrate materials. We show toughened benzocyclobutene (or BCB), Cyclotene (another form of BCB), Polyimide, Epoxy/Phenol (the traditional printed circuit board material), acrylic, and polybenzoxazole (or PBO). Each material has its own advantages and disadvantages. For example, BCB has the best dielectric constant, but suffers from a high coefficient of thermal expansion. Polyimide works well as a high temperature substrate, but suffers from elongation and moisture uptake. Epoxy/phenol is cheap and has a low elongation value, but suffers from a low glass transition temperature. PBO has good tensile strength and a low moisture uptake, but suffers from high elongation and CTE values.

Material Property	Toughened BCB	CYCLOTENE	Polyimide	Epoxy/ Phenol	Acrylic	PBO
Cure Temp (°C)	200-250	200-250	350	190	200	175-225
Tg/Dec. Temp (°C)	350	350	>350	210	180	240
Dielectric Constant	2.65	2.65	3.2	3.5	3.4	3.1
Dissipation Factor	0.002	0.001	0.002	0.02	0.03	0.009
CTE (ppm/K)	70	42	34	54	80	80
Tensile Strength (Mpa)	93	87	200	90	<50	170
Elongation	25%	8%	45%	7%	5%	80%
Residual Stress (Mpa)	24	28	34	<30	<30	25
Moisture Uptake	0.3%	0.2%	1.3%	1.5%	1.5%	0.5%

Technical Tidbit

Trace Parasitics

An important concept, both for chip design and Printed Circuit Board (PCB) design is to minimize trace parasitics. Trace parasitics come in the form of resistance, inductance and capacitance. Improving these values helps with signal integrity, precision measurements and power measurements.

An important goal during the design of the board is to minimize resistance. The parasitic resistance of a Integrated Circuit or PCB trace is directly proportional to the length of the trace, and inversely proportional to the height and width of the trace. The equation for resistance in a uniform conductive material with a rectangular cross section is:

$$R = \frac{l_{trace}}{\sigma W T}$$

where l is the length of the trace, σ is the resistivity of the material, W is the width of the trace, and T is the thickness of the trace material. Test engineers often rout ground signals as planes rather than traces because planes offer low impedance.

Inductance is another important consideration during the design of a board or IC. Minimizing inductance is important for switching high currents and testing high bandwidth amplifiers. The inductance of a trace depends on the shape and size of the trace, as well as the geometry of the signal path through which the currents flow to and from the load impedance. The equation for inductance is

$$L_\ell = \mu_o \mu_r \frac{D}{W}$$

where D is the distance between traces, W is the width of the trace, μ_o is the permeability of air, and μ_r is the relative permeability of the medium (the dielectric material in this case). We can minimize trace Inductance in the following ways:

- Minimize the area enclosed by the load current path. Lay a dedicated current return trace along side the signal trace, or use a solid ground plane as the return path for all signals.
- Route each signal trace over a solid ground plane close in the stack up, thus the load current can return underneath the trace along a path with very low cross sectional area (Minimize D).
- Make the trace as wide as is practical (Maximize W).

Capacitance is still another important trace parasitic that we need to minimize. The equation for capacitance is

$$C_\ell = \varepsilon_r \varepsilon_o \frac{W}{D}$$

where W is the width of the trace, D is the distance between traces, ε_0 is the dielectric constant of air, and ε_r is the relative dielectric constant (or permittivity) of the medium (the insulating material in the board). The value of ε_r depends on the PCB insulator material. FR4 fiberglass has a relative permittivity of about 4.5, while teflon, by contrast, has a relative permittivity of about 2.7. Therefore, teflon is superior for high frequency applications, since it leads to lower values of parasitic capacitance. Another design practice that can reduce capacitance is to add a GND plane between traces removes trace-to-trace capacitance and reduces crosstalk. SiO_2 has a relative permittivity of about 3.9, so newer chips use Low-K dielectrics where the relative permittivity might be between 2.0 and 3.0.

Ask the Experts

Q: What are Base and Metal Layers?

A: Base layers are the layers which are implemented in the silicon substrate (like source/drain implants, VT implants, NWELL layer, etc.). Metal layers obviously refer to the mask layers associated with the back end of the process (like M1, M2, M1-M2 via, etc). In the EDA process process flow base layers are taped out first and then metal layers..

Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
   a. Philosophy of Failure Analysis
   b. Flowcharts
3. Gathering Information
4. Package Level Testing
   a. Optical Microscopy
   b. Acoustic Microscopy
   c. X-Ray Radiography
   d. Hermetic Seal Testing
   e. Residual Gas Analysis
5. Electrical Testing
   a. Basics of Circuit Operation
   b. Curve Tracer/Parameter Analyzer Operation
   c. Quiescent Power Supply Current
   d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
   e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
   f. Automatic Test Equipment
   g. Basics of Digital Circuit Troubleshooting
   h. Basics of Analog Circuit Troubleshooting
6. Decapsulation/Backside Sample Preparation
   a. Mechanical Delidding Techniques
   b. Chemical Delidding Techniques
   c. Backside Sample Preparation Techniques
7. Die Inspection
   a. Optical Microscopy
   b. Scanning Electron Microscopy

8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing
13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

ISTFA 2015
International Symposium for Testing and Failure Analysis

November 1-5, 2015
Oregon Convention Center
Portland, OR, USA

Registration is available at
http://www.asminternational.org/web/istfa-2015

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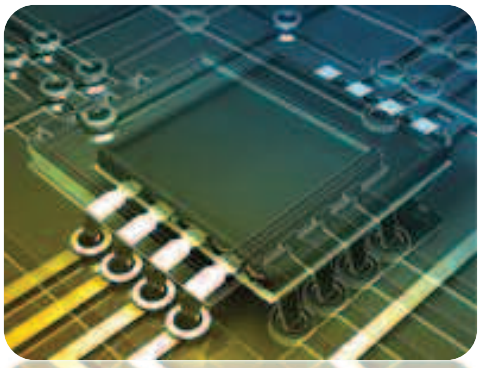
Paul Sakamoto, our VP of Business Development, will be attending and can meet with you one-on-one to discuss your training needs. Please contact him at Sakamoto@semitracks.com to schedule a meeting.



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(Click on each item for details)

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San Jose, California, USA

Failure and Yield Analysis
January 18 – 21, 2016 (Mon – Thur)
San Jose, California, USA

Failure and Yield Analysis
May 17 – 20, 2016 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
May 23 – 24, 2016 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 30 – June 2, 2016 (Mon – Thur)
Munich, Germany