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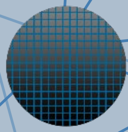

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YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

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Semiconductor Cleanroom Technology

By Christopher Henderson

In last month's Feature Article, we introduced a new series on Cleanroom Technology. In this month's Feature Article, we will continue our discussion on Cleanroom Technology with a focus on Contamination Control. We will discuss contamination, its effect on semiconductor processing, sources of contamination, and how to detect and quantify contamination levels.

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Want to take control of your learning? See Page 10

See page 14 for details on how to schedule a webinar and available topics

Without contamination control, the semiconductor industry would be unable to manufacture components, since the thin films and small feature sizes of most all devices are subject to damage or change when contamination is present. This is a broad topic, so we will distill the subject down to the major points. We will begin with an overview of the topic, followed by the effects of contamination on semiconductor processing. We will then discuss the sources of contamination, and finally, we will discuss techniques for characterization and measurement.

Let's begin with some examples. These images in Figure 1 show examples of contaminants. The images on the top row of Figure 1 show examples of particles on wafers. The three left images on the bottom row of Figure 1 show examples of residue, and the image on the bottom right in Figure 1 is a crystal defect, that was initiated due a particle on the surface of the wafer before an epitaxial deposition step.

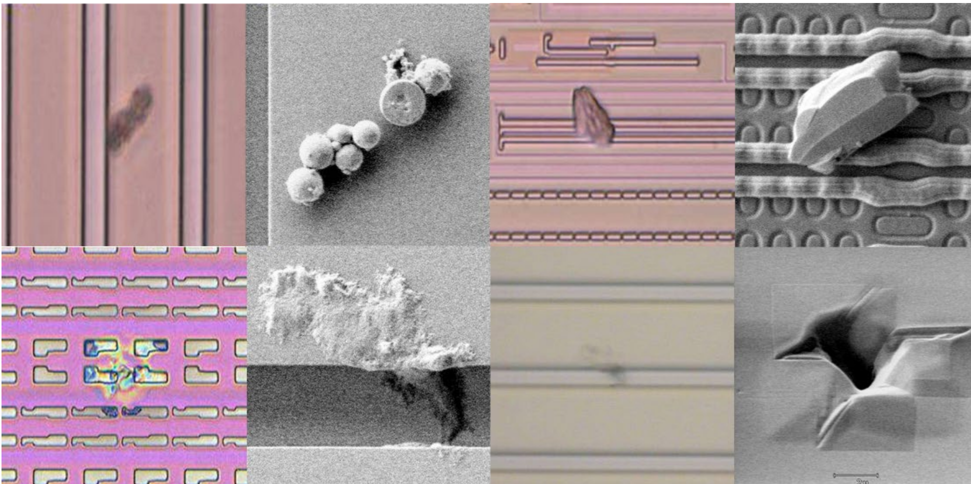
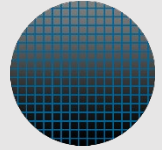


Figure 1- Examples of contamination on wafers

We know that we need the upmost in contamination control in order to achieve good device yields. It is necessary, but not sufficient in itself, as other problems like design-manufacturing interactions can also limit yield.



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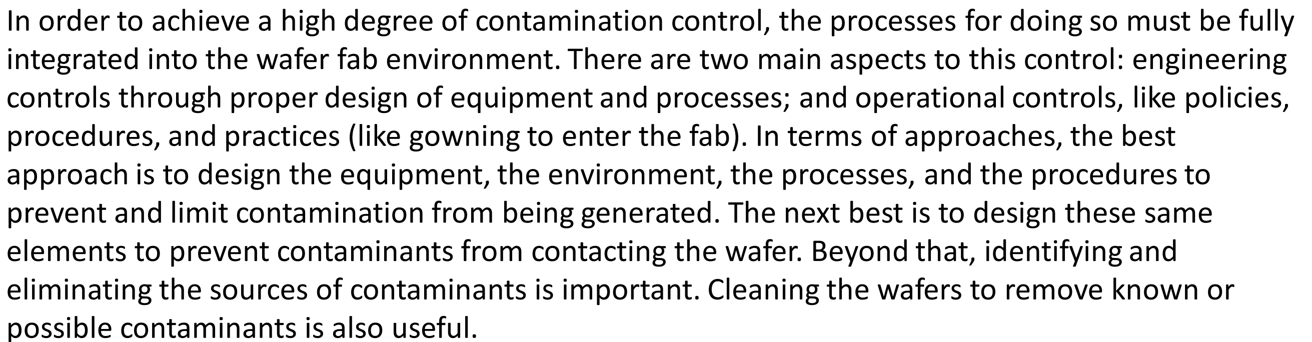


In order to achieve a high degree of contamination control, the processes for doing so must be fully integrated into the wafer fab environment. There are two main aspects to this control: engineering controls through proper design of equipment and processes; and operational controls, like policies, procedures, and practices (like gowning to enter the fab). In terms of approaches, the best approach is to design the equipment, the environment, the processes, and the procedures to prevent and limit contamination from being generated. The next best is to design these same elements to prevent contaminants from contacting the wafer. Beyond that, identifying and eliminating the sources of contaminants is important. Cleaning the wafers to remove known or possible contaminants is also useful.

We can break down contamination control into four major categories: fab environment; process fluids; equipment; and the processes themselves. Under fab environment, we need to consider air, personnel, and clean-room design and construction. Under process fluids, we need to consider water, process chemicals and process gases. Equipment is another major issue, as moving pieces can generate particles, along with wear and tear to the equipment itself. Under the actual processes themselves, we need to consider such things as handling processes, maintenance processes, cleaning processes, and host of other items can lead to contaminants as well. Contamination can take on many forms and effects. The forms of wafer contaminants include particulates, which would be discrete bits of material; films, which would be thin layers, sometimes monolayers, of materials; and traces of contaminants in molecular or atomic form, such as sodium, copper, iron, or aluminum. These contaminants can be either organic or inorganic, and the form is a critical factor for both detection and removal. From a device or integrated circuit point of view, contamination will degrade device performance, reduce the yield or degrade device reliability. Often, two, or even all three effects, can happen with contamination.

Let’s briefly discuss the effects of contaminants from a processing point of view. Contaminants can affect block and mask processes, such as etching, ion implantation, thermal oxidation, and other processes. Contaminants can impair film adhesion, such as the adhesion of metals to silicon. Contaminants can cause electrical shorts, or opens. For instance, particles can bridge between metal lines, causing a short, like we see in the image in Figure 2. Particles within metal lines can cause opens as well. Contaminants can also provide nucleation sites in deposited films, which can lead to enhanced deposition, or micro-voids in polysilicon deposition. Contaminants can also provide nucleation sites for silicon crystal defects. Finally, contaminants are sources of ionics and metallics. They can diffuse rapidly into silicon during thermal processing.

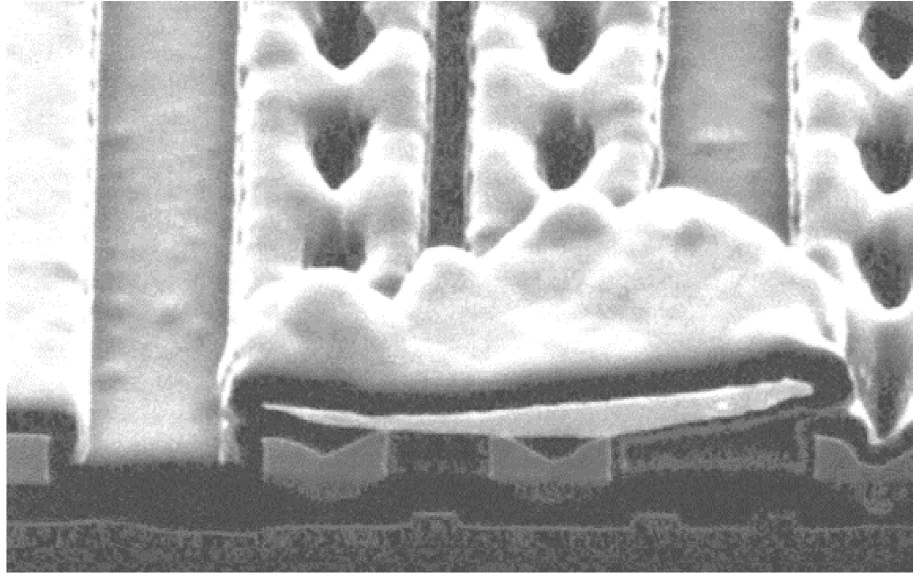


Figure 2- Example of contamination bridging between metal lines on an integrated circuit

Particle contamination levels need to remain below critical levels in order for integrated circuits to be manufactured with high yields. Particle size, count, and density all play a role. One can think of particle size in terms of critical diameter. This is a function of the technology node, and is typically around 50% of the minimum feature size. Particle count and density levels are also a function of many factors. These include: the nature of the contaminant; the minimum feature size; the chip size; the circuit complexity; the type of circuitry; and the spatial distribution of the particles. For spatial distribution, this refers to factors such as uniformity or clustering. Figure 3 shows typical limits for contamination levels for cleanroom classes as a function of the size of the particles. For example, at the 65nm technology node, the Front End Of Line processes should have a maximum particle density of approximately 0.1 particles/cm^2. Metallic contaminants, that one might find in a wafer or on a wafer surface, are also a function of many factors. The typical maximum permitted level for metallic compounds is typically less than 1 x 10^{10} atoms/cm^2.

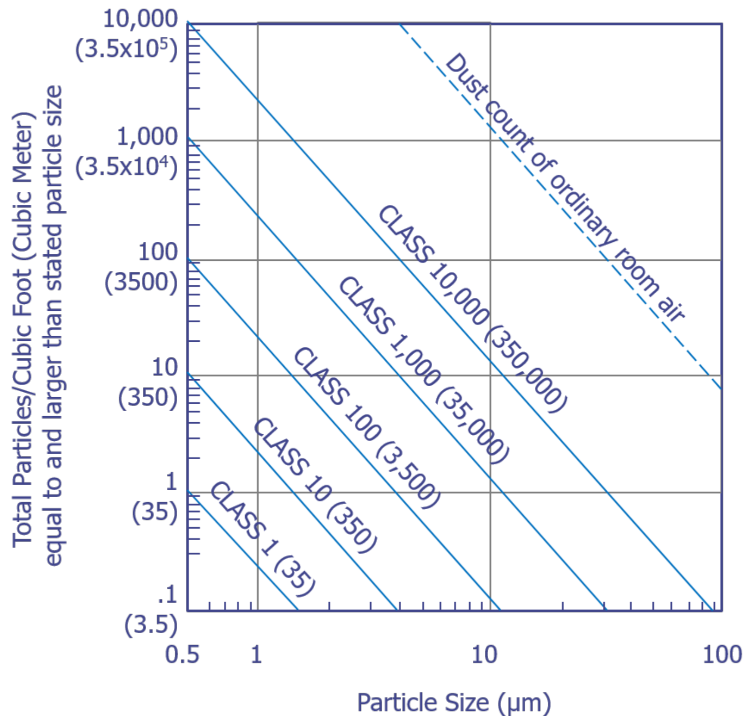


Figure 3- Typical limits for contamination levels for cleanroom classes as a function of the size of the particles

Now let's turn our attention to some sources of contaminants. One important source of contamination is the air in the manufacturing facility. Clean room technology can help reduce the airborne contamination. The degree of cleanliness is specified by the class or level of the cleanroom. For sub-micron and nanometer-level processes, the process areas need to be ISO 3 or cleaner. However, the service or chase areas can be one or two levels less clean. In contrast, room air in a standard office environment or home is greater than ISO 9. We filter the contaminants from the air in the clean room in several stages. First, pre-filters remove most of the large particles. Next, activated charcoal filters remove contaminants such as sulfur dioxide and nitrogen dioxide. HEPA or ULPA filters then provide the final cleaning process for the air. These filters are positioned above the work surface to provide laminar flow, and are designed to move large volumes of air at low velocity. HEPA filters remove better than 99.97% of particles 0.3 µm and larger, while ULPA filters remove better than 99.9995% of particles 0.1 µm and larger. We will have more to say about filtration in a later Feature Article.

Next, let’s discuss contamination that originates from personnel. Some contaminants of concern include particles like those that come from skin flakes, hair, street clothing, and even your breath, should you be a smoker. Other contaminants include alkali metals like sodium, that can come from skin oils, or road salt. Still other contaminants include metals that can be present in cosmetics. The main strategy to minimize this type of contamination is to cover yourself from head to toe with clean-room clothing. This includes a body suit, boots, a face mask, and safety glasses. The clothing is non-shedding fabric that is a densely woven polyester or Gore-tex type material. It must also be cleaned and packaged properly. This type of contamination is readily controlled by proper clothing and procedures; and through the cleanroom design itself and the Wafers In Transit, or WIT. We will have more to say about cleanroom clothing and gowning in a future Feature Article.

One major challenge with contamination is how to characterize and measure the type and level of contamination. The defect levels and impurity concentrations are very low. For example, for particle sizes of less than 10 nm, the density must be less than 0.01 particles/cm^2. Also, for example, surface metallics must be below 1 x 10^8 particles/cm^2. The device circuitry is getting smaller and ever more complex, so smaller and smaller particles can still impact the yield. Another challenge is that this monitoring needs to be done in real-time. This means that cleanrooms will use airborne particle detectors to monitor the clean room air; liquid particle detectors to monitor the process fluids like ultrapure water; gas particle detectors to monitor process gases like argon; ultrapure water resistivity monitors, and air contamination detectors, to monitor the cleanroom air for trace amounts of acids, bases, and organics. This can be critical for some advanced photolithography processes, where levels need to be down in the parts per trillion range. We show equipment that can be used for monitoring in Figure 4. There may be many other monitors that cleanrooms use to ensure the cleanroom is indeed a clean environment.

Figure 4- Monitoring equipment for cleanroom contamination

An important method for detecting contamination is the wafer inspection system. These are also known as laser, or particle, scanners, or wafer surface scanners. They are used to detect and count particles and other defects on bare silicon wafers and on blanket films on unpatterned wafers. Imaging patterned wafers with particle scanning systems for contamination can be quite difficult, as the pattern and materials properties can often confuse the software in the wafer inspection tools into thinking there are or aren't particles, when the opposite is true. These systems operate on the following concept, as shown in Figure 5. First, the system scans a laser beam across the surface of the wafer. Next, the light scatters off the wafer, and the system detects the scattered light as light point defects, sometimes abbreviated as LPD. After the system collects the light, it then amplifies and analyzes the optical information. In a modern system, the software can size the defects, based on algorithms. The main applications for these systems include tool and process qualification and re-qualification, and routine tool monitoring. The sensitivity of new tools, like the KLA Instruments Surfscan SP5, is quite good. It is typically better than 5 nanometers.

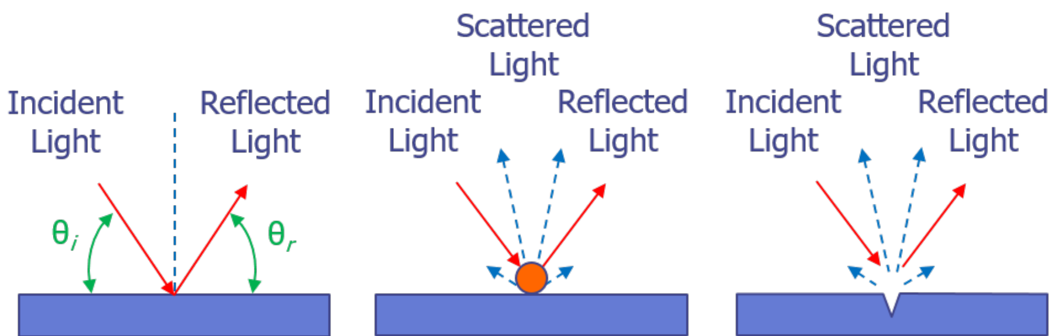


Figure 5- Concept behind laser particle, or wafer surface, scanners

Another type of wafer inspection system is the inline wafer inspection system. These systems are used to detect and characterize defects on patterned wafers. For example, these systems can be used to detect equipment and process-induced particles; process residues from etch, or photoresist strip; or chemical mechanical polishing; or from patterning and etch defects. The main application is routine monitoring of specific process steps. The principle of operation is similar to that of systems used on unpatterned wafers, but utilize a variety of optical techniques. This includes dark field illumination with laser light, where only the scattered light is visible; bright field illumination with ultraviolet or deep ultraviolet light; and dark field illumination using an electron beam for excitation. There are many challenges to this approach. First, one needs to filter out signals from device patterns. Second, one needs to account for topography, which includes three-dimensional devices like FinFETs. Third, one must account for a wide range of films; and fourth, one must be able to deal with high aspect ratio features. As such, the size of defects one can identify is somewhat larger.

For instance, the KLA-Tencor 3900 Series PWI claims a detection resolution of <10 nm for defects. These systems also contain sophisticated algorithms for filtering out pattern signals. Figure 6 shows a photo of an in-line patterned wafer inspection system from KLA Instruments. These systems are designed for a production environment; however, the speed at which these systems can inspect wafers is limited. Therefore, one cannot inspect all of the wafers at every process step.

Figure 6- KLA Instruments 9850 Patterned Wafer Inspection System

There are other methods to detect and characterize contamination. One method is to use a patterned wafer macro inspection system. These systems are variations of patterned wafer inspection tools, and provide the process engineer with a quick check for macro-level defects. The main application for this class of tool is lithography. Another method is to use a standard optical microscope. This is a fast method, but the resolution is limited. The limit of optical microscopy is one-half the wavelength of visible light. Visible light is in the range of 0.4-0.7 µm, so the resolution is approximately 0.25 µm. Another method is to use a standard scanning electron microscope, or SEM. While the throughput is quite low, the SEM does allow for very high-resolution imaging. A related method is energy-dispersive x-ray analysis or EDX. This technique works in conjunction with the SEM and provides elemental analysis of particles and contamination. All three techniques are used to review or analyze specific defects, or area defects detected by wafer inspection systems. In conjunction with these techniques, engineers may use in-situ particle monitors to quantify particle counts in process tools. These might be mounted in the tool chamber or downstream from the process chamber. They typically use a laser beam. The particles will scatter the light, and the scattered light can be analyzed. Since these techniques are slower, one cannot do this for every wafer. Therefore, engineers will use a sample plan based on statistical process control methodologies, and will include additional sampling if excursions occur.

This concludes our discussion of contamination control. In next month's Feature Article, we'll discuss cleanroom construction.

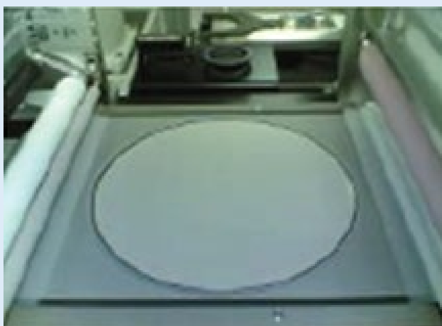
Technical Tidbit: Taper

This month's Technical Tidbit covers "taper"– the process of laminating the wafer prior to backgrinding.

Figure 1-

The loading system and cassette for the taper process

Taper system and loading system



Wafer after the taper process

In the taper process, engineers place a tape on the top side of the wafer surface to serve as a protective layer for the backgrinding process. This tape can be manufactured to be thick enough to protect not only the wafer surface, but also the bump structures, if there is a bump process used during manufacturing.

Figure 1 shows the equipment for the taper process in a series of images. The input to the process would be an un-grinded wafer. The wafers are moved into the tape machine via a cassette, as shown in the top image. For 200mm wafers, the cassette will be a traditional plastic cassette. For 300mm wafers, the cassette will be a Front Opening Shipping Box, or FOSB, as shown in the top image. The tape would then be applied to the wafer using a system like the one depicted in the center image. The type of tape will be dependent on the type of devices manufactured on the wafer. The bottom image shows an example of a taped wafer.

As an inspection step before the grinding, an operator, or an automated imaging system, will scan the surface of the taped wafer, looking for chips, cracks, signs of tape delamination, foreign material, or irregular bumps. The output of this process is a wafer that is laminated with backgrinding tape. The taped wafers would then be loaded back into the cassette system. The cassettes can be moved to the next stage of the packaging operation in the factory using a Material Transport Vehicle System, or MVTS.

Ask The Experts

Q: I was under the assumption that during Chemical Vapor Deposition (CVD), a reaction between the reactant gases and substrate occurs to form the film. Is this not the case with all CVD?

A: Your thinking is mostly correct, but I do want to make a clarification to your statement. The proper way to think about the physical behavior of CVD is that the reactant gases react with each other in the presence of the substrate to form a film; however, the substrate is not affected by the reaction. The layer would simply be deposited on the substrate, much like a layer of snow is deposited on the ground during a winter storm. All three forms of CVD: Plasma-Enhanced CVD, Low Pressure CVD, and Atmospheric Pressure CVD, exhibit this behavior. Furthermore, Atomic Layer Deposition (ALD) exhibits this behavior as well.

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Course Spotlight: EOS ESD and How to Differentiate

This is one of our public courses we are planning to hold in 2023. Stay tuned on our website for course announcements!

COURSE OBJECTIVES

With focused guidance from your instructor, you will gain insight into the following:

1. electrical overstress, the models used for EOS, and the manifestation of the mechanism.
2. the ESD failure mechanism, test structures, equipment, and testing methods used to achieve robust ESD resistance in today's components.
3. major issues associated with ESD, and explain how they occur, how they are modeled, and how they are mitigated.
4. identifying basic ESD structures and how they are used to help reduce ESD susceptibility on semiconductor devices.
5. distinguishing between EOS and ESD when performing a failure analysis.
6. estimating a pulse width, pulse amplitude, and determining the polarity of an EOS or ESD event.
7. examples of common problems that result in EOS and ESD in the manufacturing environment.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, you will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of current, relevant experience in this field. The course notes offer dozens of pages of additional reference material you can use day to day.

OVERVIEW

Electrical Overstress (EOS) and Electrostatic Discharge (ESD) account for most of the field failures observed in the electronics industry. EOS and ESD damage can at times look quite similar to each other, but the source of each, and the solution required can be quite different. This makes it important to be able to distinguish between the two mechanisms. The semiconductor industry needs knowledgeable engineers and scientists to understand these issues. ***EOS, ESD, and How to Differentiate*** is a 2-day course that offers detailed instruction on EOS, ESD, and how to distinguish between them. This course is designed for every manager, engineer, and technician dealing with these failures, analyzing field returns, determining impact, and developing mitigation techniques.

What constitutes a good ESD design? What types of devices reduce ESD susceptibility? We'll explore these questions and look into how to design new ESD structures for a variety of technologies.

1. **Overview of the EOS Failure Mechanism:** learn the fundamentals of EOS, the physics behind overstress conditions, test equipment, sources of EOS, and the results of failure.

2. **Overview of the ESD Failure Mechanism:** learn the fundamentals of ESD, the physics behind overstress conditions, test equipment, test protocols, and the results of failure.

3. **ESD Circuit Design Issues:** learn how circuits are designed to protect against ESD damage. This includes MOSFETs, diodes, off-chip driver circuits, receiver circuits, and power clamps.

4. **How to Differentiate:** learn how to tell the difference between EOS and ESD by simulating damage and interpreting pulse widths, amplitudes and polarity.

5. **Resolving EOS/ESD on the Manufacturing Floor:** we'll go over a number of common problems and their origins.

COURSE OUTLINE

Day 1

1. Introduction
    a. Terms and Definitions
    b. ESD Fundamentals
    c. EOS Fundamentals

2. Electrical Overstress Device Physics
    a. Sources of EOS
    b. EOS Models
    c. Electrothermal Physics

3. Electrostatic Discharge Device Physics
    a. ESD Models
    b. ESD Testing and Qualification
    c. ESD Failure Criteria
    d. Electrothermal Physics
    e. Electrostatic Discharge Failure Models
    f. Semiconductor Devices and ESD Models
    g. Latchup

4. EOS Issues in Manufacturing
    a. Charging Associated with Equipment
        i. Testers
        ii. Automated Handling Equipment
        iii. Soldering Irons
    b. Charge Board Events
    c. Cable Discharge Events
    d. Ground Loops/Faulty Wiring
    e. Voltage Differentials due to High Current
    f. Event Detection

Day 2

5. ESD Protection Methods
    a. Semiconductor Process Methods
    b. MOSFET Design
    c. Diode Design
    d. Off-Chip Drivers
    e. Receiver Networks
    f. Power Clamps

6. Differentiating Between EOS and ESD
    a. EOS Manifestation
    b. ESD Manifestation
    c. Circuit considerations
        i. Chip level
        ii. System level
    d. Simulating ESD
    e. Simulating EOS

7. EOS/ESD Design and Modeling Tools
    a. Electrothermal Circuit Design
    b. Electrothermal Device Design
    c. ESD CAD Design

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