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YOUR QUARTERLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY



Transfer Molding

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In this quarter's Feature Article, we continue our series on Transfer Molding. Transfer Molding is one of the more common steps in semiconductor packaging, and provides protection for the sensitive semiconductor components and packaging interconnect. We will continue our discussion of transfer molding by focusing on electrical characterization tests used to assess mold compounds.

The epoxy resin mold compound can be thought of in terms of a capacitor. We show a diagram of the capacitor structure in Figure 1 at the left. Therefore, we can use an inductance-capacitance-resistance, or LCR, meter or impedance analyzer for dielectric characterization. The frequency of the applied voltage is changed, and the current generated would be recorded. The current amplitude and phase shift can then be converted to generate a permittivity value. The impedance is equal to the voltage divided by the current, and the capacitance is equal to one over the quantity two pi times the frequency impedance. The permittivity is then equal to the capacitance divided by the geometrical capacitance. We show the electrical properties of the capacitor in Figure 1 on the right. The diagram that shows I_C as a function of V is the permittivity of the material. The vertical axis represents the imaginary part, and the horizontal axis represents the real component.

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- Wafer Fab Processing
- IC Packaging Technology
- Failure and Yield Analysis
- EOS,ESD and How to Differentiate

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Figure 1- Capacitor structure (left), and electrical properties (right).

The dielectric properties of the epoxy resin mold compound become important, especially when dealing with high voltage components. We show some data in Figures 3-6 that characterize our example epoxy resin mold compound – the Sumitomo G720 epoxy resin mold compound. These measurements were taken on an older system, a TA Instruments DEA 2970, like we show in Figure 2. The current system from TA Instruments that will allow you to perform this type of experiment is the ARES-G2 with the Dielectric Thermal Analyzer accessory. The dielectric measurements were made in a frequency range from 1 to 100,000 Hz over a temperature range from 30°C to 300°C with a heating rate between 1 and 10°C per minute.

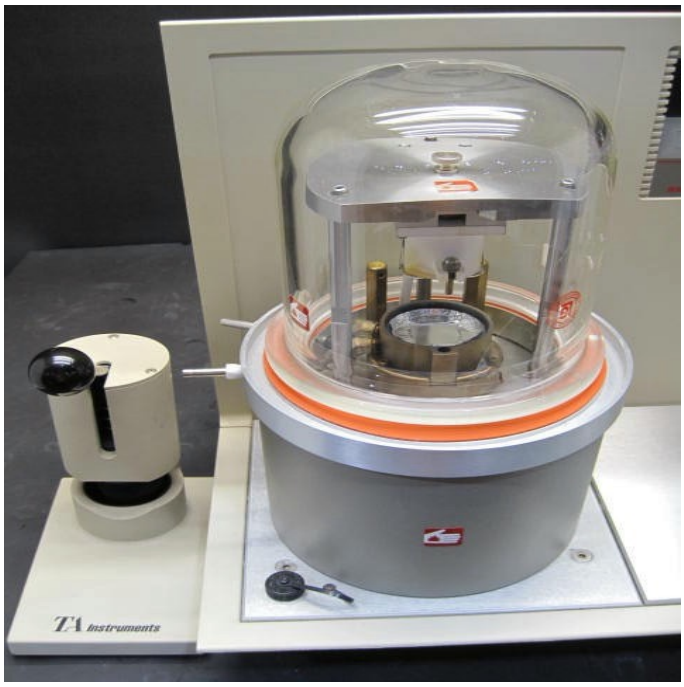


Figure 2- Photograph of the TA Instruments DEA 2970 Dielectric Analysis System.

Figure 3 shows some typical measurement results from dielectric thermal analysis. We show the temperature profile on the left, and a tangent of δ plot on the right that corresponds to the temperature profile. Tangent δ, sometimes referred to as a loss tangent, in this plot is the ratio between the imaginary part and the real part of permittivity. Referring to the diagram in the upper right portion of the figure, it is the green arrow divided by the red arrow.

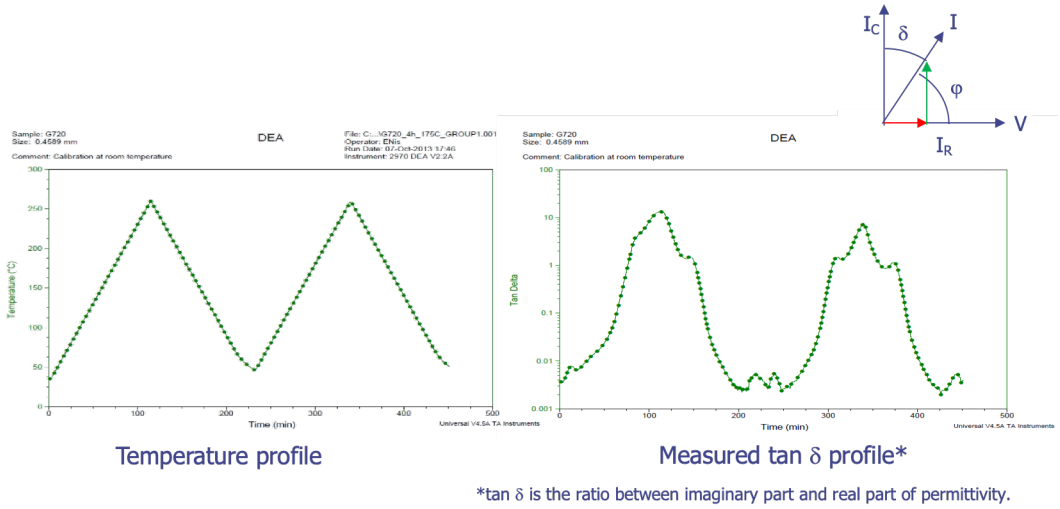


Figure 3- Typical measurements from dielectric thermal analysis.

Depending on the Post Mold Cure conditions, epoxy resin mold compound will have a different final set of electrical properties. Each time our example epoxy resin mold compound reaches temperatures that exceed 200°C, some portion of it cures. We see this in the Differential Scanning Calorimetry plot in Figure 4 on the left. The graph in Figure 4 on the right shows the log of the tangent of δ as a function of temperature for two epoxy resin mold compounds with different post mold cure conditions. Notice that as the curing temperature increases, the tangent of δ becomes much larger, indicating that the epoxy resin mold compound's permittivity becomes much less a function of the real component, or leakage due to the resistance of the material, and much more a function of the imaginary component, or the leakage due to the capacitance of the material.

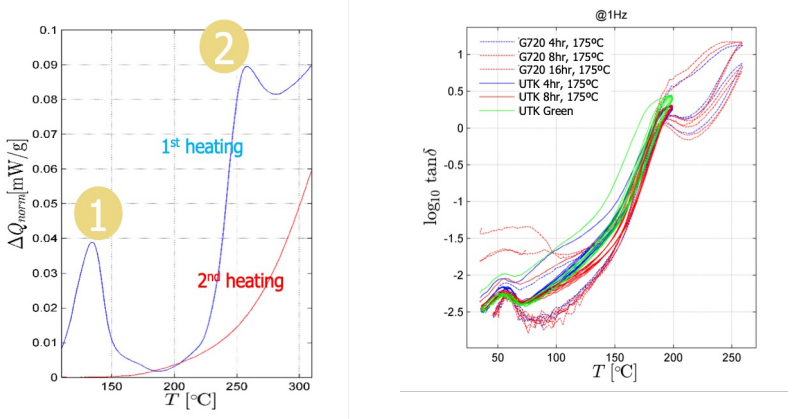


Figure 4- Differential Scanning Calorimetry Plot (left), and log of tangent δ vs. temperature (right).

Figure 5 shows additional data on the influence of post mold cure conditions on the dielectric properties. In this example, the green curves represent a device with no epoxy resin mold compound, the blue curves represent a device that underwent a post mold cure at 175°C for 4 hours, and the red curves represent a device that underwent a post mold cure at 175°C for 8 hours. Notice that the loss tangent δ at 10 hertz decreases with time as the temperature is cycled (highlighted by the red arrow). The green sample has the highest losses (highlighted with the red box).

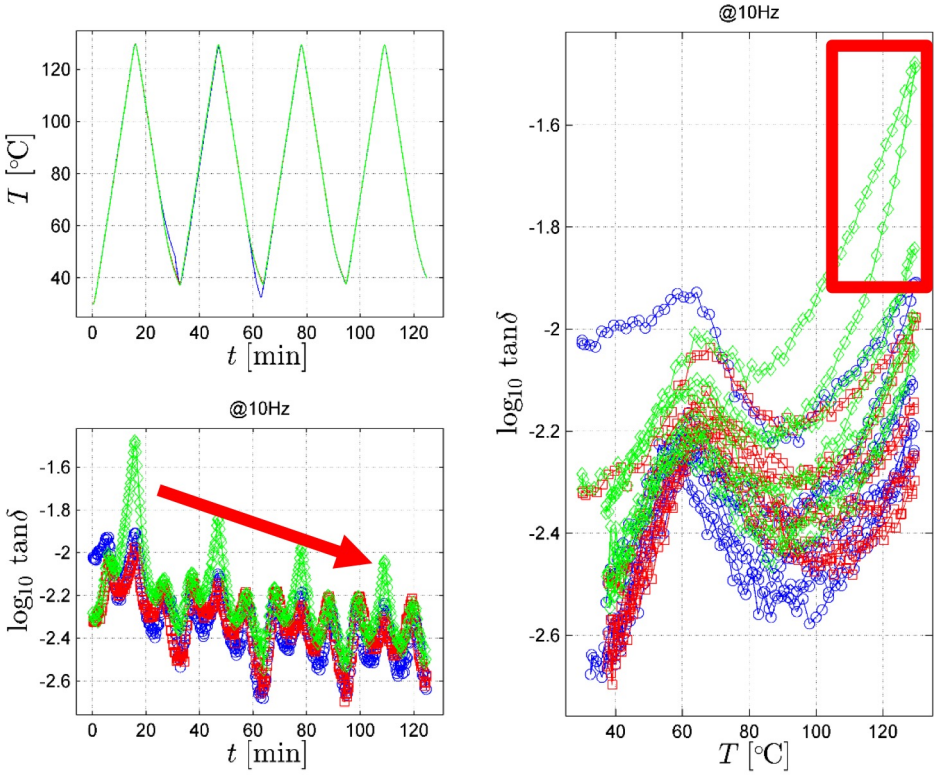


Figure 5- Plots showing the effect of the post mold cure conditions for the Sumitomo mold compound.

In Figure 6, notice that there is a clear polarization peak at 120°C at 1 kHz. This relaxation, or slight decrease in the loss tangent (highlighted by the upper arrow in the left graph), is associated with the high temperature cure portion of the Sumitomo epoxy resin mold compound curing process. We can remove this relaxation by heating the material (highlighted by the lower arrow in the left graph). Notice in the graphs on the right, if we just heat to 130°C, the peak remains the same (highlighted by the upper arrow in the right graph). However, the peak goes away after we ramp up to 310°C and then come back down (highlighted by the lower arrow in the right graph).

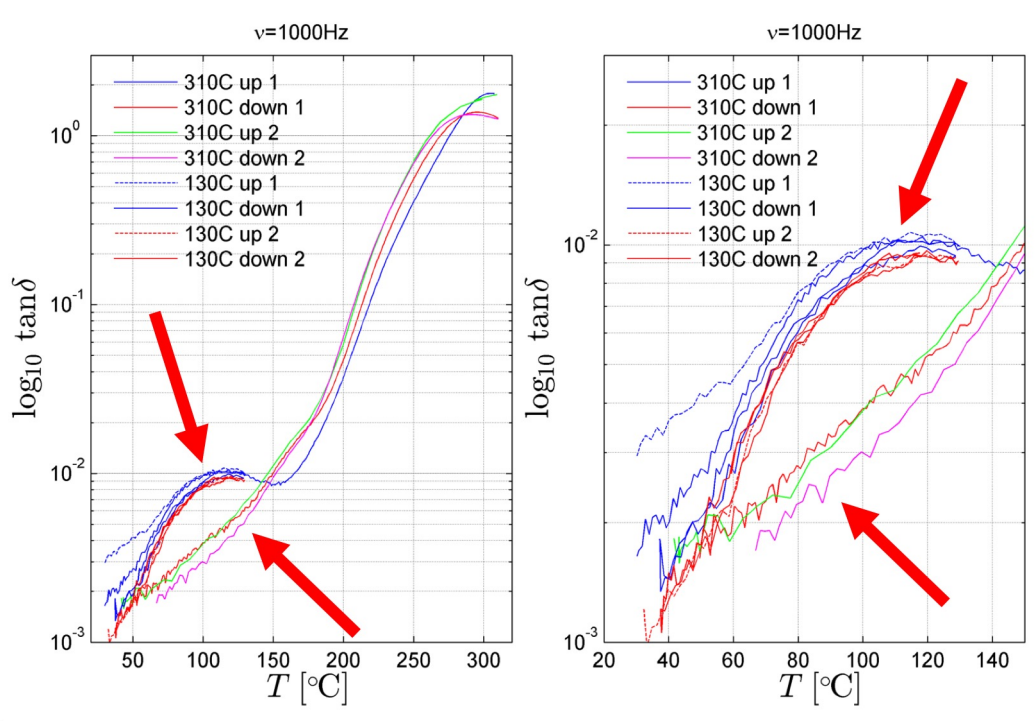


Figure 6- Plots showing the effect of the post mold cure conditions for the Sumitomo mold compound.

In next quarter's Feature Article, we will continue our discussion of transfer molding by continuing our discussion of the electrical properties of mold compounds and additional characterization tests used to assess mold compounds.

Technical Tidbit – Electrical Signal Transmission through Vias and Bumps

In this month's Technical Tidbit, we will discuss Via and Bump technologies. Via and Bump technologies play an important role in advanced package configurations. Most people think of solder bumps and copper pillars when it comes to bump technology, but vias (including Through Silicon Vias and Through Mold Vias) are also an important category as well.

For basic circuit simulation (e.g., SPICE), a sub-100 µm a via or bump can be modeled using passive RLC components. This is sometimes referred to as the Lumped Element Equivalent Circuit Model (see Figure 1). However, because solder bumps and vias can bridge an Integrated Circuit (IC) to a package substrate or interposer, their transition must also capture the surrounding geometry.

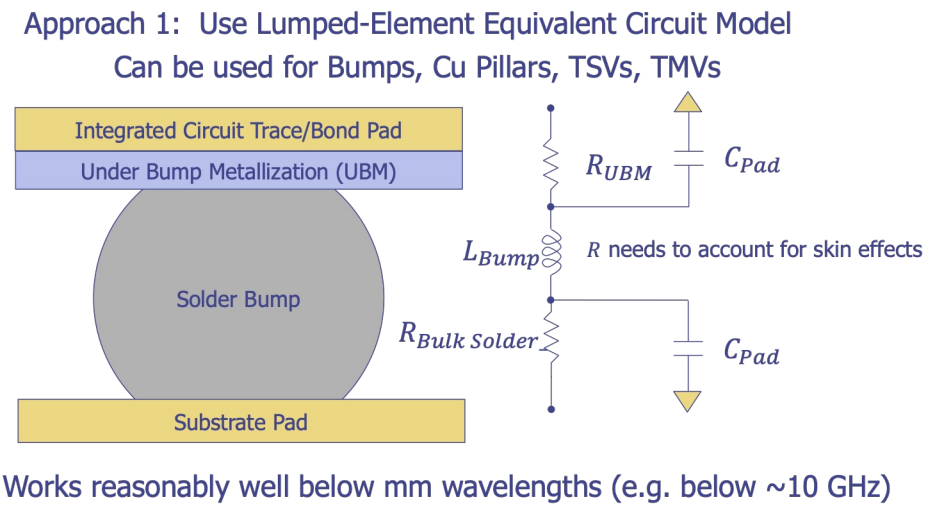


Figure 1- Diagrams illustrating the Lumped-Element Equivalent Circuit Model.

The first factor is resistance, which includes the resistance of the bump or via, and the Under Bump Metallurgy, or UBM layer (R_{Bump} and R_{ubm}). Solder alloys (e.g., Sn-Ag-Cu) have higher resistivity than pure copper. The model must also account for the UBM layer and localized intermetallic compounds (IMCs). At higher frequencies, skin effect forces the signal to the outer perimeter, artificially inflating AC resistance.

The second factor is inductance (L_{bump}). Solder bumps and vias exhibit minor parasitic inductance (typically 10 to 50 pH depending on bump or via height and aspect ratio). Though tiny, at data rates above 28 Gbps, this inductance acts as a low-pass filter, limiting the cutoff frequency ($\omega_c \approx R/L$).

The third factor is capacitance (C_{pad}). The physical landing pads on the die and the substrate create parasitic capacitance to nearby ground planes. This causes a localized drop in characteristic impedance (Z_0).

As data rates enter the millimeter-wave spectrum, lumped RLC circuits lose accuracy because the electrical size of the interconnect transition approaches the signal's wavelength. Engineers utilize 3D Field Solvers (e.g., Ansys HFSS, Keysight ADS/EMPro, or CST Studio Suite) to accurately capture propagation physics. We show an example of such a simulation in Figure 2.

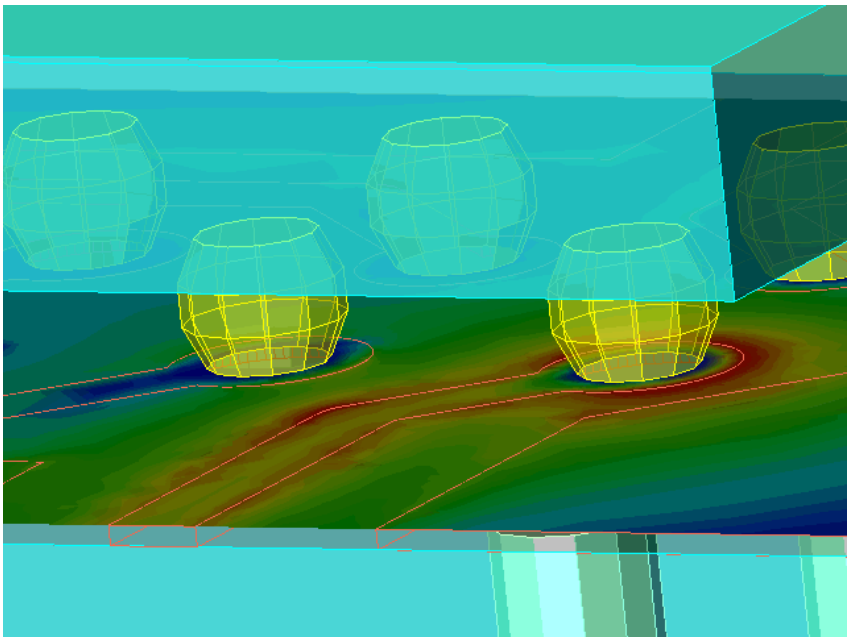


Figure 2- Model of a network of bumps connecting a semiconductor chip with a substrate.

Generally, there are some common key simulation objectives. The first is S-Parameter Extraction (S_{11} & S_{21}). The solvers calculate Return Loss (S_{11}) to track signal reflections and Insertion Loss (S_{21}) to capture attenuation across a broadband range (e.g., 0–100 GHz). The second is current crowding. Models show that electricity does not flow evenly through the bump. It dramatically bunches, or "crowds", at the sharp corner entry point from the horizontal trace into the vertical bump, which alters high-frequency impedance and accelerates electromigration. The third is Crosstalk & Isolation. In dense arrays, such as those seen with Fine-Pitch Flip-Chip Ball Grid Array (FC-BGA) and 3D Heterogeneous Integration schemes, the fields of neighboring signal bumps couple together. Field solvers map out the required ratio of ground-shielding bumps to signal bumps (e.g., Ground-Signal-Ground configurations) to enforce isolation.

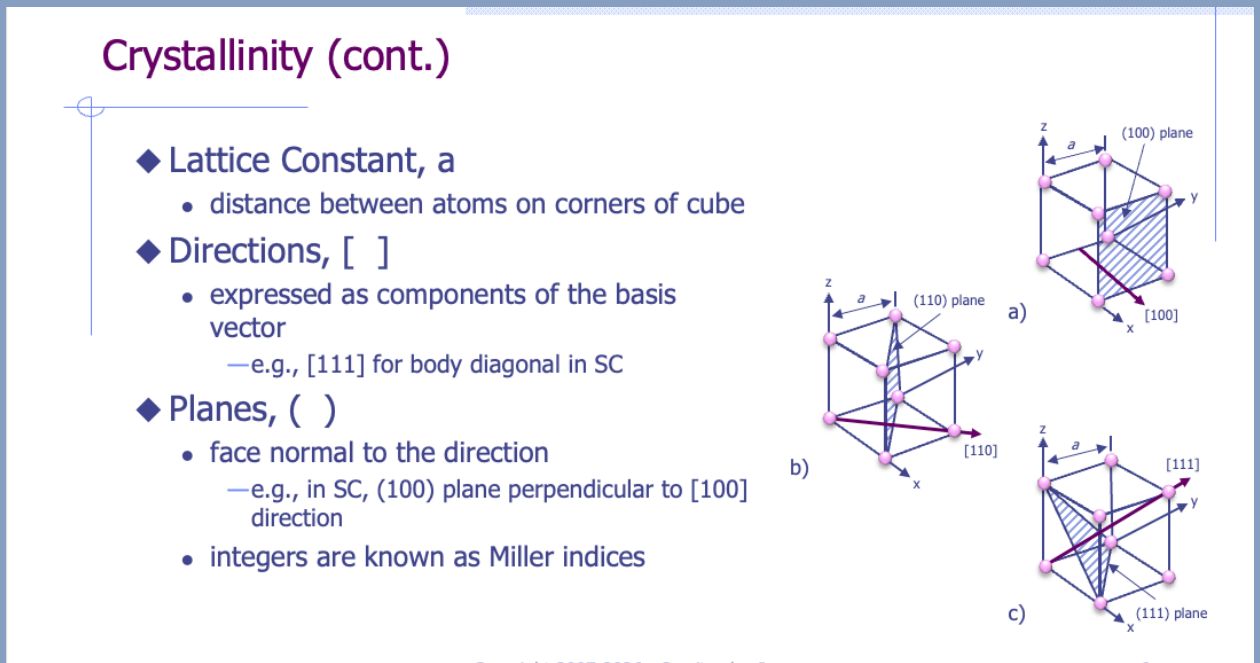
In conclusion, there are two main approaches for modeling electrical signal transmission through bumps and vias: using a standard simulation tool like SPICE in conjunction with the Lumped Element Equivalent Circuit Model, and 3D Full-Wave Electromagnetic Modeling with specialized software. Increasingly, 3D Full-Wave Electromagnetic Modeling is necessary, due to the high operating frequencies and complex signal routing configurations associated with products in the AI era.



Ask The Experts

Q: While watching a video in the Online Training System about ingot manufacturing, I had a question which came to my mind, that relates to my daily routine (I make samples for cross-section SEM imaging). This might be an elementary level question, but I would like to ask it. The more experienced engineers in the fab usually ask me to slice the wafer 45 degrees to the notch, along the grain when making samples. In school I learned that the notch on the wafer represents the certain lattice direction of Silicon crystal, but I am still not clear which direction the notch represents. Is it perpendicular or parallel to the ingot slice? If the explanation might get to a deeper level (like lattice structure), can you recommend to me any book or reference that would give me a better understanding? I would appreciate your help. Since I did not have a degree in electrical engineering or device physics, when I joined my company, I don't have this background. I really appreciate the help from your videos in the Online Training System about major production processes and basic device physics.

A: Thank you for your question, and here is the answer. The wafer manufacturer mechanically grinds flats or a notch into the ingots before a semiconductor manufacturer receives them. As you noted, the primary flat or notch is oriented to a specified crystal direction. For example, on a (100) wafer: the flat perpendicular to [110] direction, and the notch points in the [110] direction. To determine why to slice the wafer at 45 degrees to the notch, you need to understand the crystal structure of the silicon. Below is a screenshot from our Online Training System that shows this crystal structure.



Course Spotlight: SEMICONDUCTOR RELIABILITY AND PRODUCT QUALIFICATION

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms, and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability; assessing the impact of new materials; dealing with limited margins, and other factors. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Semiconductor Reliability and Product Qualification is a 4-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants will learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product. This skill building series is divided into four segments:

1. **Overview of Reliability and Statistics.** Participants will learn the fundamentals of statistics, sample sizes, distributions and their parameters.

2. **Failure Mechanisms.** Participants will learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, and others.

3. **Qualification Principles.** Participants will learn how test structures can be designed to help test for a particular failure mechanism.

4. **Test Strategies.** Participants will learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The course will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.

2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.

3. The course will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.

4. The course will offer a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.

7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

DAY 1

1. Introduction to Reliability
    a. Basic Concepts
    b. Definitions
    c. Historical Information

2. Statistics and Distributions
    a. Basic Statistics
    b. Distributions (Normal, Lognormal, Exponent, Weibull)
    c. Which Distribution Should I Use?
    d. Acceleration
    e. Number of Failures

DAY 2

1. Overview of Die-Level Failure Mechanisms
    a. Time Dependent Dielectric Breakdown
    b. Hot Carrier Damage
    c. Bias Temperature Instability
    d. Electromigration
    e. Stress Induced Voiding
    d. BEOL Dielectric Reliability

2. Package Level Mechanisms
    a. Moisture/Corrosion
        i. Failure Mechanisms
        ii. 3Models for Humidity
        iii. T_{ja} Considerations
        iv. Static and Periodic stresses
        v. Exercises
    b. Thermo-Mechanical Stress
        i. Models
        ii. Failure Mechanisms
    c. Chip-Package Interactions
        i. Low-K fracture
    d. Through Silicon Via Reliability
    e. Thermal Degradation/Oxidation

DAY 3

1. Board Level
    a. Package Attach (Solder) Reliability
        i. Creep/Sheer/Strain
        ii. Lead-Free Issues
        iii. Electromigration/Thermomigration
        iv. MSL Testing
    b. Board Level Reliability Mechanisms
        i. Interposer
        ii. Substrate

2. Use Condition Failure Mechanisms
    a. Electrical Overstress/ESD
    b. Radiation Effects

3. Test Structures and Test Equipment

4. Developing Screens, Stress Tests, and Life Tests
    a. Burn-In
    b. Life Testing
    c. HAST
    d. JEDEC-based Tests
    e. Exercises

DAY 4

1. Calculating Chip and System Level Reliability

2. Developing a Qualification Program
    a. Process
    b. Standards-Based Qualification
    c. Knowledge-Based Qualification
    d. MIL-STD Qualification
    e. JEDEC Documents (JESD47H, JESD94, JEP148)
    d. AEC-Q100 Qualification

3. JEDEC Tests

4. Exercises and Discussion

Upcoming Courses:

Semiconductor Reliability and Product Qualification – February 1-4, 2027 (Mon.-Thurs.) | Cambridge, UK – $2,095 until Mon. Jan. 18

Advanced CMOS/FinFET Fabrication – February 16-17, 2027 (Tues.-Wed.) | Dresden, Germany – $1195.00 until Tues. Jan. 26

Wafer Fab Processing - February 22-25, 2027 (Mon.-Thurs.) | Dresden, Germany – $2,095 until Mon. Feb. 1

IC Packaging Technology – March 3-4, 2027 (Wed.-Thurs.) | Munich, Germany – $1195.00 until Wed. Feb. 10

Failure and Yield Analysis - March 8-11, 2027 (Mon.-Thurs.) | Munich, Germany – $2,095 until Mon. Feb. 15

EOS, ESD and How to Differentiate - May 19-20, 2027 (Wed.-Thurs.) | San Jose, CA - $1,195 until Wed. Apr. 28

Failure and Yield Analysis - May 24-27, 2027 (Mon.-Thurs.) | San Jose, CA - $2,095 until Mon. May 3

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!