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Transfer Molding

By Christopher Henderson

In this article we will provide an overview of the transfer molding process. The transfer molding process is the most common method for packaging components, although in recent years engineers have begun using other techniques. We'll discuss how to perform transfer molding, and issues associated with the process.

This section is divided into five sub-sections. We'll begin with an overview of the molding process, followed by an overview of the equipment and materials. Next we'll discuss the materials properties that are important to the mold compound. We'll end with a couple of statements about future mold compound materials.

Molding is the process of encapsulating the device in hard plastic material. Transfer or injection molding is the most widely used molding process in the semiconductor industry because of its capability to mold small parts with complex features. In this process, the molding compound is first preheated prior to its loading into the molding chamber (see Figure 1). After pre-heating, the mold compound is forced by a hydraulic plunger into the pot where it reaches the melting temperature and becomes fluid. The plunger continues to force the fluid mold compound into the runners of the mold chase. These runners serve as canals where the fluid mold compound travels until it reaches the mold cavities, which contain the leadframes or BGA substrates for encapsulation. In conventional equipment, cavities that are nearest the runner gates get filled up first. The first cavity experiences the highest filling velocity. The fill-

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ing velocity decreases as the first cavity is filled. Subsequent cavities are filled with increasing velocities until the last cavity, which has the second highest filling velocity. As such, the first and last cavities are most prone to wiresweeping and die paddle shift.

Figure 2 shows an example of the molding equipment. The machinery is a combination of a pressure system to force the two halves of the mold together, and a heating system to bring the mold compound to a liquid state so that it will flow through the runners and to the chip assemblies.

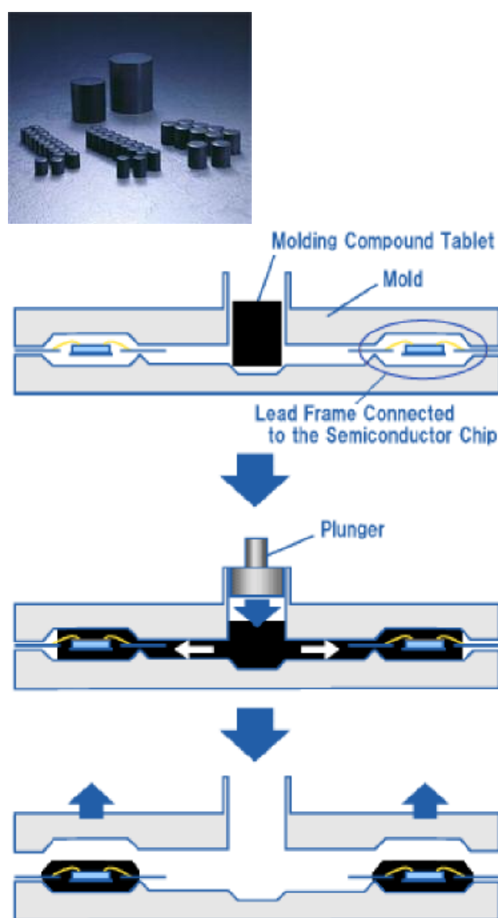

Figure 1. Overview of mold transfer process.

Figure 2. Example of molding equipment.

Mold compound is a combination of materials. They combine to form a protective plastic to cover or encapsulate a semiconductor device or integrated circuit. Mold compound consists of resin, filler particles, typically crushed quartz or quartz beads, a catalyst, flame retardants like organobromines or organophosphates, an adhesion promoter and a mold release agent. These materials can be purchased as a pressed cylinder or puck, like we show here.

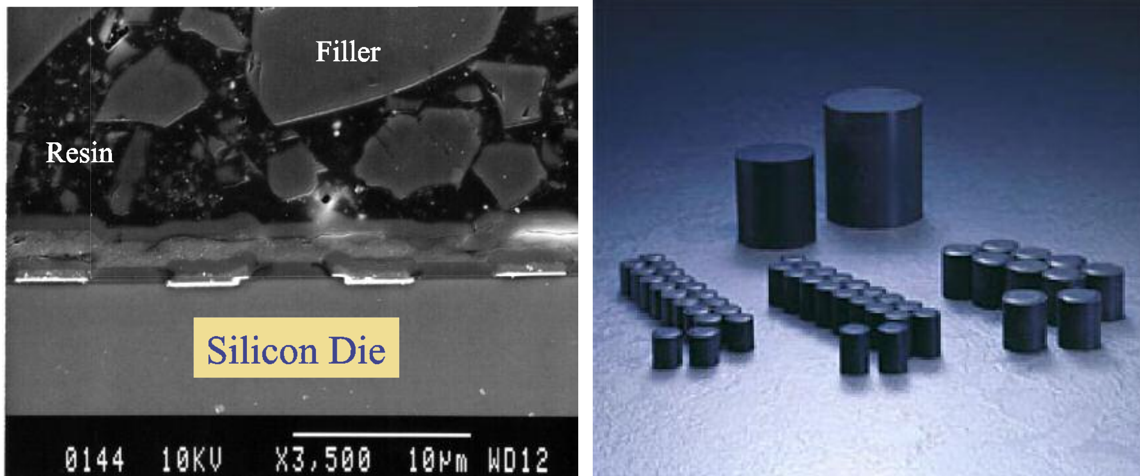

Figure 3. Cross-section of a typical mold compound (left) and encapsulant molding materials (right).

The mold compound forms a protective sealant for the die and wire bonds. This is not a hermetic seal, but it does provide a level of protection against moisture and corrosion. In the semiconductor industry, transfer molding is the primary method. Upper and lower plates come together to form the mold cavity for the semiconductor package. We show an example of such a plate in the image on the right.

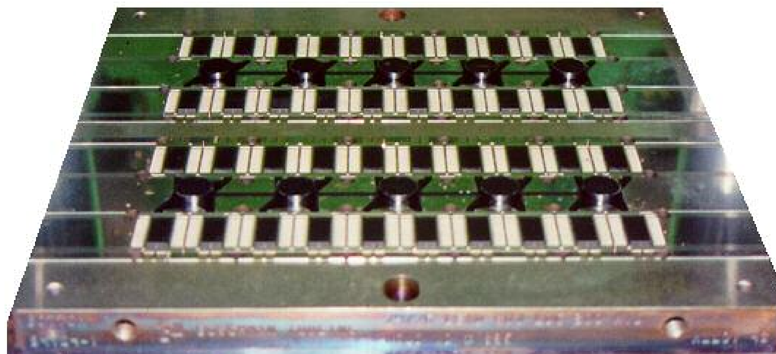

Figure 4. Mold transfer plates.

Since the flow and curing process can be somewhat slow, the manufacture of high volume products requires parallel processing. Engineers achieve this through arrayed substrate strips, where they arrange the devices in an array so that numerous devices can be encapsulated simultaneously. One issue with this approach is warping in the strip. This needs to be minimized for equipment fixturing and tools that require planar surfaces. Re-enforcement through stabilizer strips can help prevent warping.

Increased wire density and wire length in stack die packages make molding stack packages more difficult than conventional single-die packages. For example, different layers of wire bond loops, subjected to varying amounts of drag force, can result in differences in wire sweep. This increases the possibility of wire shorts.

Furthermore, the various gaps between the components make it more difficult to remove all of the voids and achieve a balanced flow with the mold fluid.

Mold compound material development, runner gate design, and wire layout optimization are required to achieve better yield in molding.

Low-viscosity compounds, smaller filler size compounds, and slower transfer speed show improved wire sweep.

A top runner gate design is more desirable than a corner gate in reducing wire sweep, especially for long wire applications. A lateral worked loop trajectory also reduces mold sweep by pre-deforming the wire in anticipation of the sweep direction. Molding experiments showed decreased wire sweep with this loop trajectory. On average, the molding sweep was reduced by nearly 50%. Folded forward looping can also reduce molding sweep by reducing excess wire in the loop and by eliminating heat-affected zone (HAZ) by folding the heat-affected region.

HAZ is weakest region along wire that is subject to mold compound sweep.

After the mold injection occurs, one must cure the mold compound to complete the polymer cross-linking that hardens the material. This is typically done at temperatures around 175°C for an hour. Warpage can be a problem during both the mold injection and the curing process, so engineers in recent years have invested some time and effort modeling these effects

Selecting the package materials, and in particular, the mold compound, is an important piece of the package design and engineering process. We know that the package will possibly contain a lead frame, and or wires, solder bumps or pillars. We know that the package might contain a polymer substrate. There will of course be one or more semiconductor chips, and in some instances, there may be ceramic materials. Therefore the choice of mold compound that can best hold these materials together is a critical

task. One major factor is stress. We will discuss the effect of stress in more detail later in this section.

New materials and materials processing technologies will be needed to meet the technology requirements for the packaging and assembly of next generation devices. With the mechanically weaker ultra low-κ dielectrics in the device, compatible underfill materials properties in the flip chip package will lessen the risk for interface stress damage to the dielectric layer. The developments of potential solutions (such as wafer level packaging and interconnect and system in package technologies) will require materials and materials processing innovations beyond what is available today.

Researchers are busy developing new infrastructure for packaging materials. This corresponds to requirements coming from environmental issues such as Lead-free and Halogen-free government directives, and requirements on next generation devices utilizing Low-κ or Ultra Low-κ. For the above implementation, the molding compound and package substrate, which are the principal materials to determine package reliability level, have to be modified considering the thermomechanical stress management to adapt for Lead-free, Halogen-free, and Low-κ/ultra-low-κ packaging. The essential property for mold compound and package substrates for Lead-free applications would be how they maintain sufficient heat resistance during solder reflow from a material characteristic point of view.

Lead:	**Mercury:**	**Cadmium:**	**Hexavalent Chromium:**	**Poly Brominated Biphenyls:**	**Poly Brominated Diphenyl Ethers:**
Pb	Hg	Cd	Cr+6	PBB	PBDE

Table 1. Partial list of banned substances

Going forward, there are several challenges regarding packaging materials, and molding compound in particular. The industry needs molding compounds that can be used for low-profile multi-die packages. They need materials that will be compatible with low dielectric constant materials now in use on chips, as well as the newer lower dielectric constant materials in development. These materials need to address gate leakage associated with charge storage in the halogen-free materials mandated by newer regulations. They also need to address metal particle contamination that leads to delamination and assembly problems. Beyond that, these new materials need to have the same or better performance than the existing materials, and need to be characterized for high frequency use.

In conclusion, we discussed the mold transfer process to encapsulate microelectronic components. This is an important aspect of the assembly process, since the package provides both environmental and mechanical protection. We discussed the molding process, the equipment and the materials, as well as some important materials properties associated with the mold compounds. The industry is just beginning to understand how to model these packages, so further characterization will be needed to understand the existing materials and their behavior as a package encapsulant. New materials will require even more study as issues like low-k dielectrics and green packaging materials receive increased attention.

Technical Tidbit

Dynamic Mechanical Analysis

A physical test commonly performed on packaging materials is Dynamic Mechanical Analysis. This technique provides insight into the viscoelastic behavior of materials. Scientists perform Dynamic Mechanical Analysis, or DMA, at room temperature, over temperature ranges, and at various frequencies. The instrument applies pressure to the sample and records changes in its change in volume or height.

This is a notional dynamic mechanical analysis temperature ramp test. Here we are looking at the change in modulus as a function of temperature. The blue curve represents the storage modulus or the energy built up as elastic energy, and the dashed red curve represents the loss modulus or the energy dissipated as heat. There are four regions in this plot, a glassy region at low temperatures, a transition region, followed by a rubbery plateau region, and a terminal region at the highest temperatures.

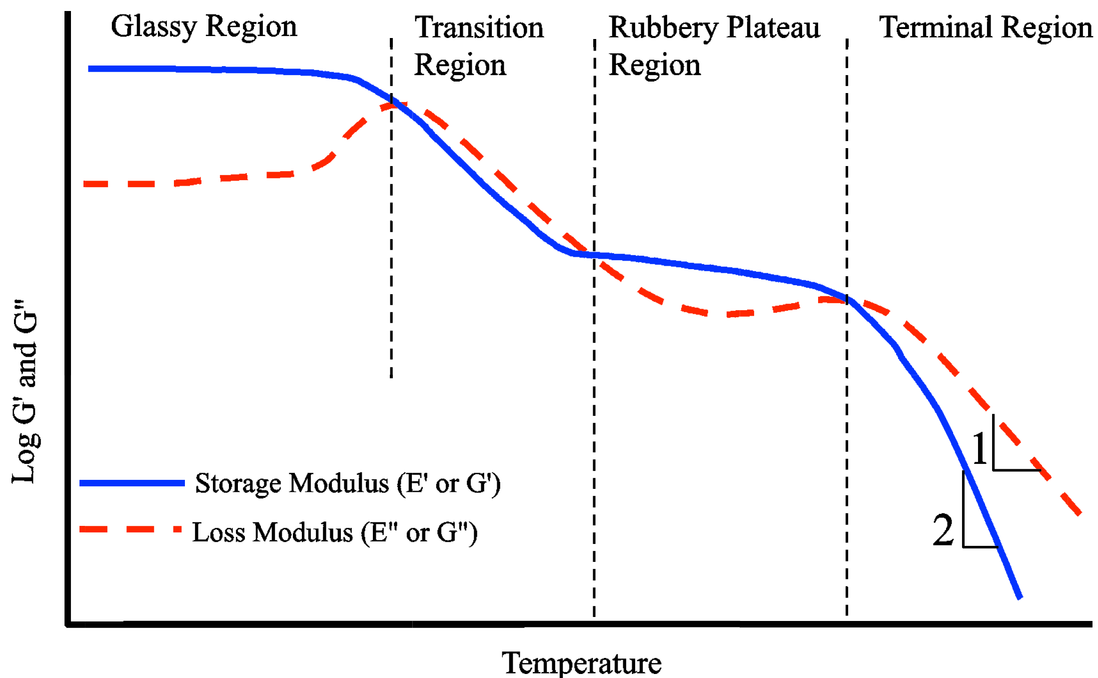

Figure 1. Typical DMA temperature curve.

Scientists use DMA to evaluate thermal coefficients of expansion and glass transition temperatures. By using frequency-based measurements, one can also gain insight into the polymer molecular motions, and determine if the glass transition temperature is dependent on strain rate as well.

Ask the Experts

Q: Are muons a threat to computing systems? Should I be concerned about them when I formulate reliability plans for our components?

A: The short answer is "Yes," but the answer is somewhat more nuanced. Yes, muons can be a problem. Muons are charged subatomic particles with a mass of approximately 200 electrons. Although their cross-section is not very large and they not as common as alpha particles, their ability to deposit charge and disrupt electrical operation is substantial, much more so than alpha particles. However, as devices scale down, this problem appears to be lessening somewhat. A good place to learn more about their effects on circuitry is through recent papers at IRPS and NSREC. I would encourage the reader to start with the Vanderbilt paper presented in 2011 at IRPS.

Chris Henderson will be presenting a tutorial on Failure Analysis of 3-Dimensional Packages on November 5 at the

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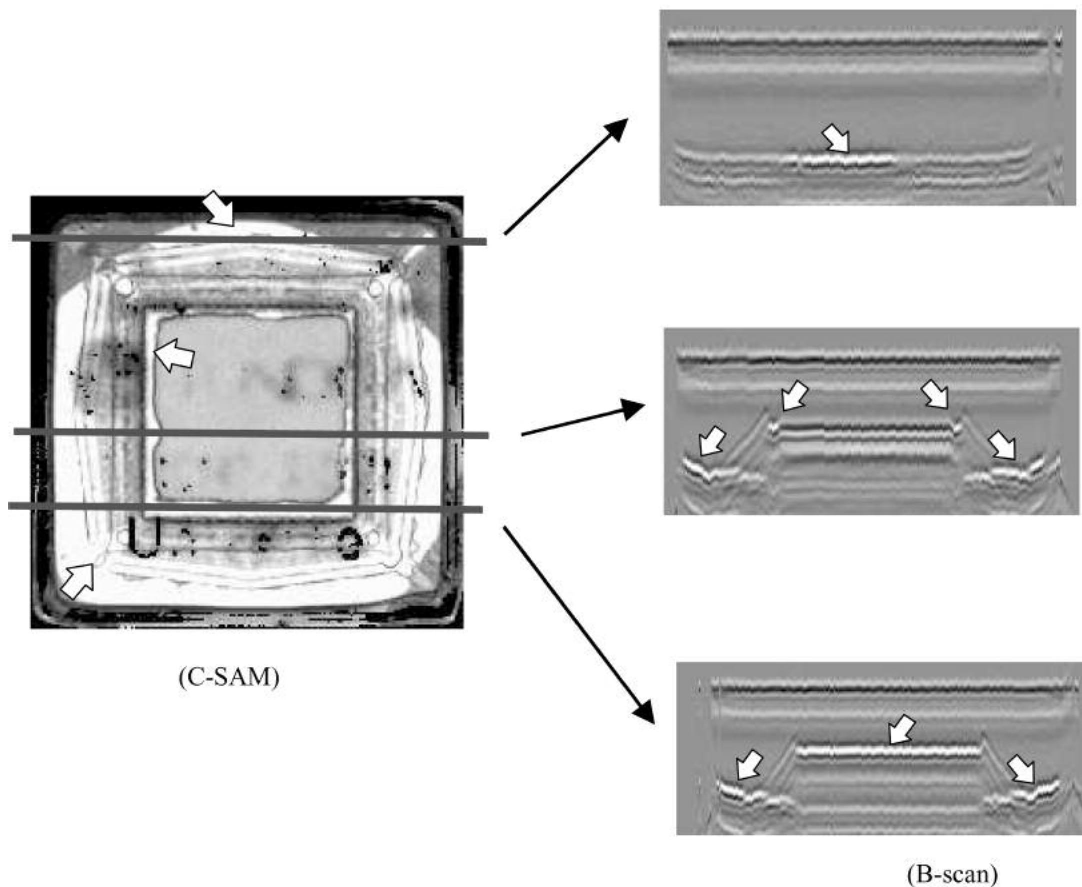
Spotlight on our Courses: Acoustic Microscopy Webinar

Acoustic Microscopy has grown in importance and use over the past 25 years. Because it is non-destructive, it is ideal for use in package-level failure analysis, reliability studies, and assembly process control. If you are interested in attending this webinar, or if you are interested in having this done as an in-house course for your staff, please feel free to contact us at (505) 858-0454, or at info@semitracks.com.

WEBINAR OVERVIEW

This webinar will provide an overview of scanning acoustic microscopy and its uses for semiconductor and electronics failure analysis. Scanning acoustic microscopy (SAM or C-SAM as it is sometimes called) is a non-destructive technique that can help localize delaminations, interface problems, examine thermomechanical and popcorn mechanism problems, and provide quality control to manufacturing/assembly processes. We will discuss how the technique works, the basic equipment for



performing the technique, and more importantly, how to interpret the images. Image interpretation is the biggest challenge with SAM, so we will delve into the issues associated with image formation, package materials and structure, and how to examine data. This webinar is a must for failure analysis engineers and technicians, reliability engineers, quality control engineers, and product engineers who read reports with this data.

WEBINAR OUTLINE

1. Introduction and Overview
2. Physics of Acoustic Microscopy
    a. Sound Behavior in Materials
    b. Reflections and Phase Difference
3. Equipment
    a. Acoustic Microscope Systems
    b. Transmission mode, A-mode, B-mode, C-mode
    c. Transducers
4. Signals, Images, and Interpretation
    a. Package Structure
    b. Package Materials
    c. Signal Formation
    d. Image Formation
    e. Dealing with signal reflections, beam spreading, etc.
    f. MIL-STD 883 Method 2030
    g. Example Images
5. Conclusions
6. Question and Answer Period

Visit Semitracks at booth 511 at the

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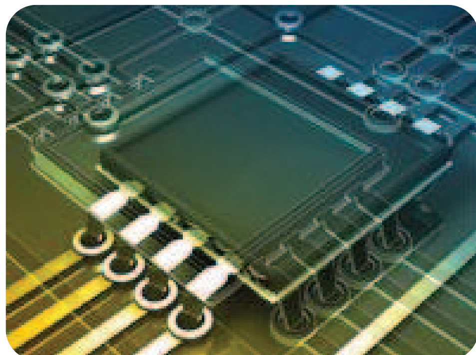

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If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

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(Click on each item for details)

IC Packaging Metallurgy
October 15 – 16, 2012 (Mon – Tue)
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IC Packaging Metallurgy
October 18 – 19, 2012 (Thur – Fri)
Melaka, Malaysia

Semiconductor Reliability
October 17 – 19, 2012 (Wed – Fri)
Kuala Lumpur, Malaysia

EOS, ESD and How to Differentiate
November 7 – 8, 2012 (Wed – Thur)
San Jose, California

Polymers in Electronics/FTIR
November 7 – 8, 2012 (Wed – Thur)
San Jose, California

Semiconductor Reliability
January 23 – 25, 2013 (Wed – Fri)
San Jose, California

Failure and Yield Analysis
January 28 – 31, 2013 (Mon – Thur)
San Jose, California

Upcoming Webinars

(Click on each item for details)

X-Ray Radiography
September 17, 2012 (Mon) • 11:00 A.M. EDT

Acoustic Microscopy
October 8, 2012 (Mon) • 11:00 A.M. EDT

Critical Topics ESD/Latchup Design
November 19, 2012 (Mon) • 11:00 A.M. EST