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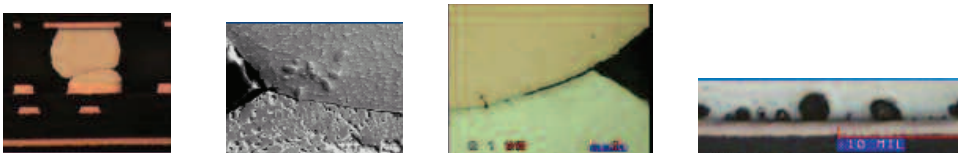
InfoTracks

Semitracks Monthly Newsletter

Lead Free Solders—General Issues Part 3

By Christopher Henderson

In addition to materials properties, there are other issues that can affect the performance of lead-free solders (Figure 19).



Solder non wetting | Backward compatibility | Poor socket wetting | Planar micro voids

Figure 19. Material and assembly process variation impacting solder joint reliability margin.

One issue is wetting. In order for the solder to make good contact to the pads on the PCB and the package, it must wet to both surfaces. Some factors that affect wetting include warpage in the PCB and package, pad contamination, oxidation of the solder paste, and a reflow process that is not optimized. Another issue is backward compatibility. There can be insufficient melting of the lead-free solder balls if they are used on a board that contains components that require a eutectic lead-tin solder process. The eutectic process requires a temperature around 215°C, while the lead-free process requires a temperature closer to 250°C. Another issue associated with wetting is a poor wetting angle. A poor wetting angle can concentrate stress near the interface, leading to crack initiation and propagation

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during thermal shock. Finally, micro voids at the interface can reduce the fatigue margin, leading to early failure of the solder joint during thermal cycling.

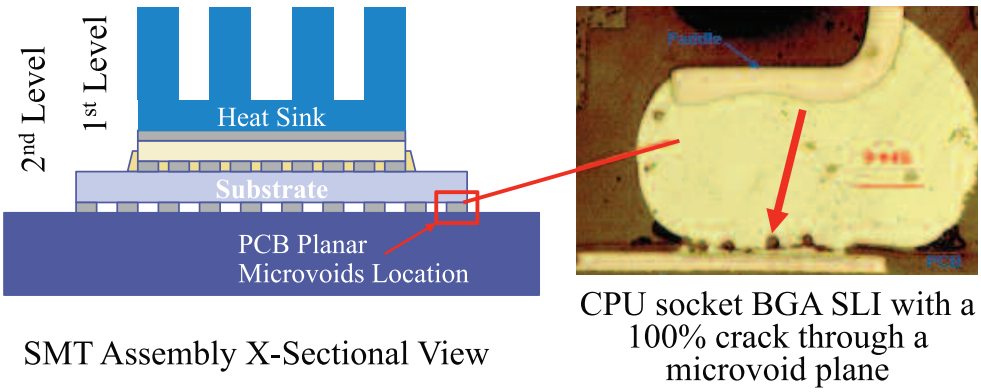


Figure 20. Diagram showing location where planar micro voids form (left) and cross-section optical image (right).

Let's discuss planar micro voids in more detail for a minute (Figure 20). This phenomenon has been observed at the interface between the substrate and the printed circuit board. The substrate acts as an interposer which spreads the pads to a larger pitch and geometry, allowing easier assembly at the board level. The voiding occurs at the solder interface to the copper pad on boards with an immersion silver finish. The image on the right shows the voiding occurring at the interface.

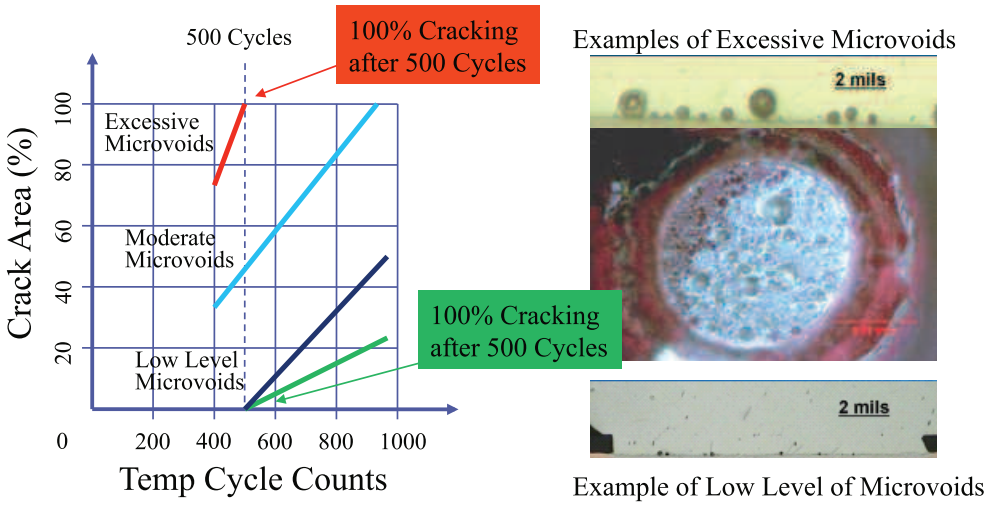


Figure 21. Planar microvoids reduce the SLI reliability margin.

The voids reduce the reliability of the solder joint by introducing locations where cracks can initiate and propagate. The graph on the left of Figure 21 shows that solder joints with a high number of microvoids fail more quickly than those with a low number of microvoids. To analyze this problem and

other solder joint interface problems, engineers will sometimes use a technique called red dye penetrant—or dye and pry—to highlight the problem. The red dye penetrates voids and cracks that are exposed to the outside environment, providing contrast when looking at a failed interface like we see in the image on the right.

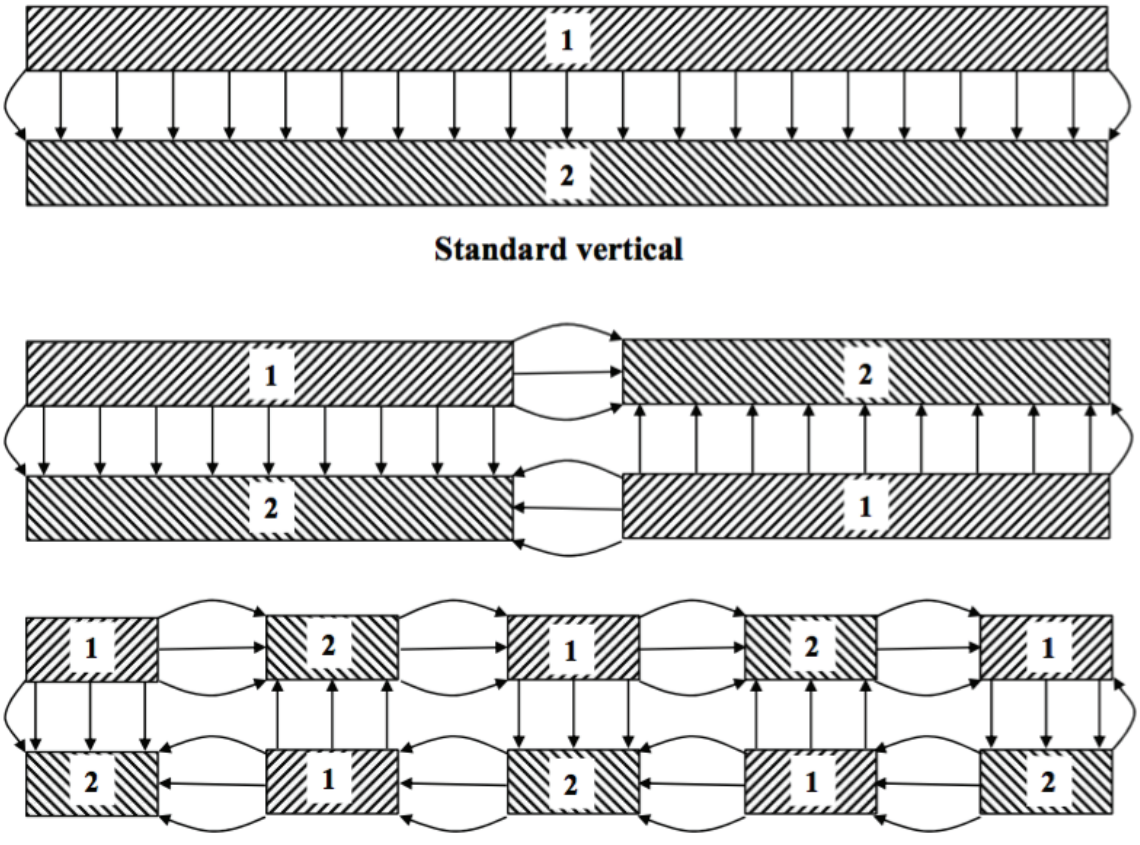
There are still some significant gaps in the evaluation and characterization process for lead-free solders. The industry needs common test methods and metrology to determine the reliability of lead-free solder joints. Most companies are still using internally-developed techniques and procedures. This makes it difficult to compare components across the industry. The industry also needs a standard for characterizing pad craters on printed circuit boards, and needs to standardize on a common test methodology for reliability characterization. As the use of lead-free solders grows, organizations like JEDEC will likely begin to address these gaps.

In conclusion, the industry has performed an extensive amount of reliability characterization for lead-free solders at both the package and board levels. In general, lead-free solders will pass the basic reliability requirements for most applications, but there are some issues that can reduce the reliability margin. This includes materials sensitivities and variation in the surface mount process. Lead-free packages have improved fatigue performance, but the mechanical margin is lower than for standard eutectic lead-tin solders. Lead-tin solders are more pliable and impart less stress to the board and package. Finally, the industry needs to converge on a standard test method and metrology procedures to allow industry-wide comparisons.

Technical Tidbit

Lateral Flux Capacitor

For our technical tidbit this month, we will discuss a structure that is not used often in chip design, but can be quite useful—the lateral flux capacitor.



Standard vertical

Vertical and lateral flux capacitors

Sl

In a lateral, or a flux capacitor, designers take advantage of the horizontal or lateral capacitance opportunities in a structure. We show some examples in the illustration here. In the middle and lower rows in the drawing, the design enhances the lateral capacitance between adjacent conductors. This illustration is for two metal levels, but one could conceivably use additional layers. In these examples, lines "1" are connected together to form terminal 1, and lines "2" are connected together to form terminal 2.

A few additional comments regarding the lateral flux capacitor are in order. The Lateral-Flux Capacitor, or LFC as some engineers refer to it, does not require added complexity in the design and layout process. One can use the existing metal layers, and simply create the structure through the appropriate layout commands. The LFC exhibits excellent VCC, TCC, and Q- factors, which makes it quite useful in precision and high-speed analog circuits. For the same area, the LFC provides a higher capacitance than the standard MOS or other types of capacitors. However, to be efficient, the LFC requires at least five metal levels on the chip, two or three for routing, and two or three for the LFC. One important drawback to the LFC has to do with technology progress. Engineers typically want to lower the capacitance in the metal interconnect to enhance performance and improve signal integrity, and they do this by using low-K dielectrics. However, switching to low-K dielectrics for the Back End Of Line (BEOL) makes the design more difficult.

Ask the Experts

Q: What is folded forward looping?

A: Folded forward looping is a wire bonding technique to help reduce wire sweep, or the movement of the wires during the mold injection process. Folded forward looping eliminates a weak region in the wire known as the Heat Affected Zone (HAZ). Just above the ball bond, the wire bonder folds the wire back on itself, creating a loop and eliminating the HAZ region. This makes the wire less susceptible to wire sweep. This picture shows an example of this.

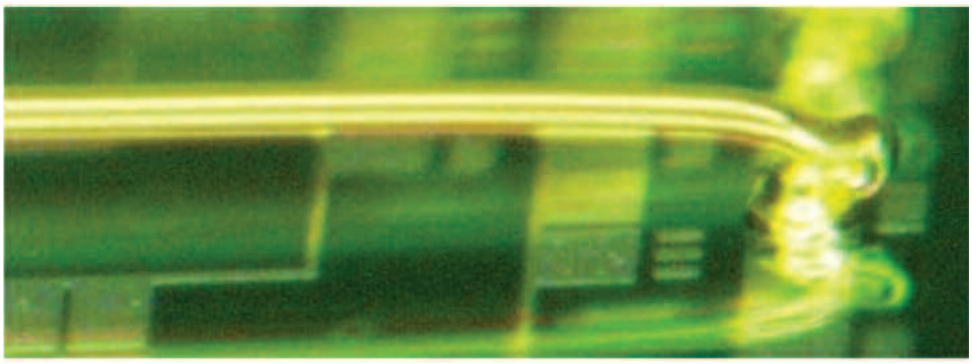


Image courtesy Kulicke and Soffa.

Spotlight: Introduction to Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Introduction to Processing*** is an online course that offers an overview look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we summarize the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

Registrants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into four segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Registrants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing and packaging/assembly came to the point where they are today. Registrants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Registrants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.
4. **Current Issues in Assembly and Packaging.** Registrants learn how packaging is a key enabler for semiconductor components. They also learn why we are seeing an explosion of different packaging types.

COURSE OBJECTIVES

1. This course will provide participants with an overview of the semiconductor industry and its technical issues.
2. Registrants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. Registrants will understand the basic concepts behind basic assembly and packaging steps.
4. This course will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
5. Registrants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.
6. Registrants will understand how processing, reliability, power consumption and device performance are interrelated.
7. egistrants will be able to understand processing steps for CMOS, BiCMOS, and bipolar technologies.
8. This course will provide an introduction to the packaging process and discuss the fundamental drivers behind the current developments in packaging.

COURSE OUTLINE

Wafer Fab Processing

Courses

1. Starting Material - Bulk Silicon Process
2. Wafer Specifications and Defects
3. Epitaxial Growth Process
4. Deposition
5. Oxidation
6. Diffusion
7. Ion Implantation
8. Dry Etching Processes
9. Wet Etching Processes
10. Chemical Mechanical Planarization
11. Lithography - Introduction
12. Lithography - Resolution
13. Lithography - Resists
14. Lithography - Subwavelength Issues
15. LOCOS and STI
16. Salicide and BEOL

Documents

1. Lithography - Introduction

Videos

1. Chip Fabrication Process
2. Micronas Wafer Fab

Assembly and Packaging

Courses

1. Assembly and Packaging Processes Introduction
2. Package Types
3. Package Design Principles
4. Dicing
5. Leadframes
6. Lead Finish and Trim - Solder Ball Attach
7. Wire Bonding
8. Die Attach
9. Transfer Molding
10. Bump Processes
11. Substrates
12. Underfills
13. Singulation

Videos

1. Packaging Overview Video

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

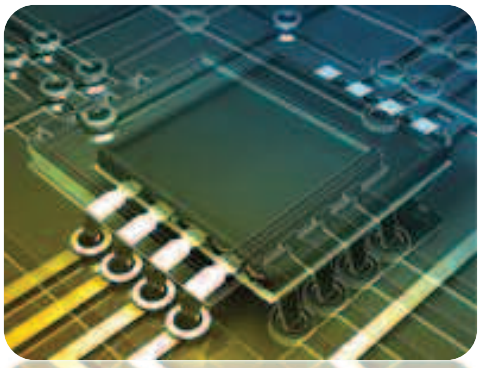
Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).

ISTFA/2017

International Symposium for Testing and Failure Analysis

November 5-9, 2017
Pasadena Convention Center
Pasadena, CA, USA

Registration is available at
https://register.rcsreg.com/r2/istfa2017/ga/top.html



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Semiconductor Reliability / Product Qualification
September 18 – 21, 2017 (Mon – Thur)
Portland, Oregon, USA

IC Packaging Design and Modeling
September 25 – 26, 2017 (Mon – Tue)
Dallas, Texas, USA

IC Packaging Technology
September 27 – 28, 2017 (Wed – Thur)
Dallas, Texas, USA

Failure and Yield Analysis
March 19 – 22, 2018 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability / Product Qualification
March 26 – 29, 2018 (Mon – Thur)
Portland, Oregon, USA

Failure and Yield Analysis
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Wafer Fab Processing
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 16 – 19, 2018 (Mon – Thur)
Munich, Germany