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YOUR QUARTERLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Transfer Molding

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In this quarter's Feature Article, we continue our series on Transfer Molding. Transfer Molding is one of the more common steps in semiconductor packaging, and provides protection for the sensitive semiconductor components and packaging interconnect. In this article, we will discuss the equipment and parameters used for the transfer molding process.

Figure 1 shows an example of the molding equipment. The machinery is a combination of a pressure system to force the two halves of the mold together, and a heating system to bring the epoxy resin mold compound to a liquid state so that it will flow through the runners to the chip assemblies.

Figure 1- Image of an "Auto Mold" transfer molding system from Towa.

WHAT'S INSIDE?

Want to take control of your learning? See page 9

Upcoming Courses:

- Si Photonics Technology and Applications
- Failure and Yield Analysis
- Wafer Fab Processing
- Defect Based Testing
- Reliability and Product Qualification
- EOS, ESD and How to Differentiate

See page 14 for more details

Figure 2 shows two examples of molding plates. The image on the left is an upper plate for an SOT-style package, and the image on the right shows both the upper and lower plates for a second type of SOT package. The upper and lower plates come together to form the mold cavity for the semiconductor package.

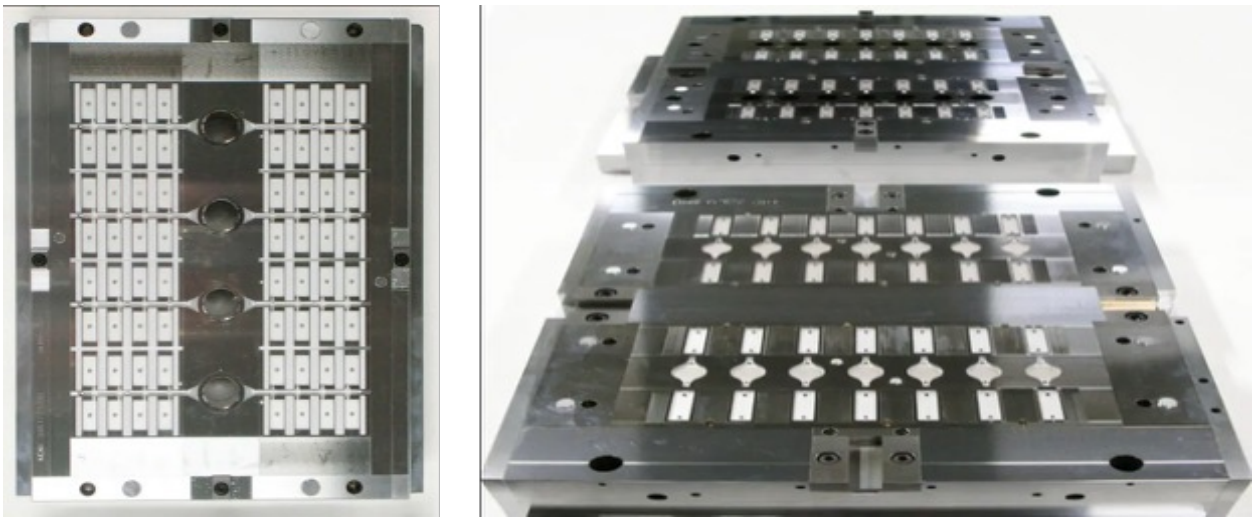


Figure 2- Upper molding plate for an SOT-style package (left), and upper and lower molding plates for a second type of SOT package (right).

Since the flow and curing process can be somewhat slow, the manufacture of high-volume products requires parallel processing. Engineers achieve this through arrayed substrate strips, where they arrange the devices in an array so that numerous devices can be encapsulated simultaneously. One issue with this approach is warping in the strip. This needs to be minimized for equipment fixturing and tools that require planar surfaces. Re-enforcement through stabilizer strips can help prevent warping. In Figure 3 we show some examples of arrayed substrate strips.

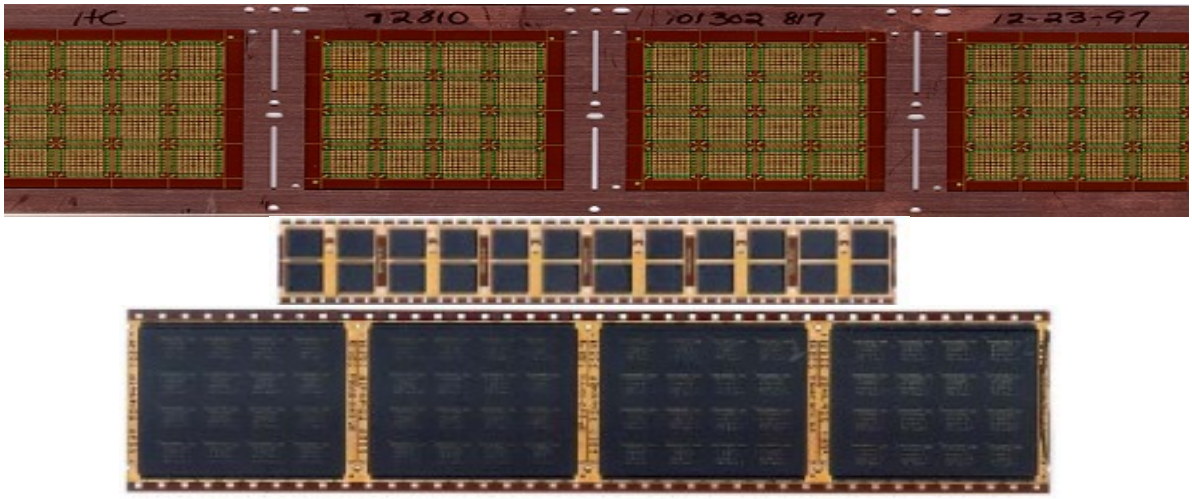


Figure 3- Examples of array substrate strips. An array substrate strip prior to chip attachment and molding (top). A small array substrate strip after the molding process (middle). A larger array format substrate strip after the molding process (bottom).

Here we list the typical parameters for the molding process:

- The preform preheat temperature is typically between 85 and 100ºC.
- The preform preheat time is between 5 and 25 seconds.
- The mold temperature is typically between 170 and 190ºC.The molding pressure is between 500 and 1200 pounds per square inch.
- The transfer time for the mold is typically 15 to 20 second in a convention mold system, and 5 to 10 seconds in an automated molding system.
- The cure time in the molding system is between 60 and 90 seconds.
- The post mold cure temperature is typically between 165 and 185ºC.
- The post mold cure time is typically 4 to 6 hours.

After the molding process in the molding system, the packages undergo a post mold cure. This is performed after de-gating and culling to ensure the epoxy resin mold compound is fully cured. The post mold cure condition is typically around 175ºC for 4 to 6 hours, excluding the ramp up and ramp down time for the oven. In Figure 4, we show a graph that indicates the degree of curing that has occurred based on the steps in the molding process. While the majority of the curing takes place by the end of the molding process, the post mold cure accomplishes the final 5 to 10% of the curing process. For certain types of gate leakage sensitive devices, the post mold cure time may be longer to eliminate the gate leakage at high voltage conditions. The longer time helps to redistribute any charge that has built up on the surface of the die due to the transfer molding process.

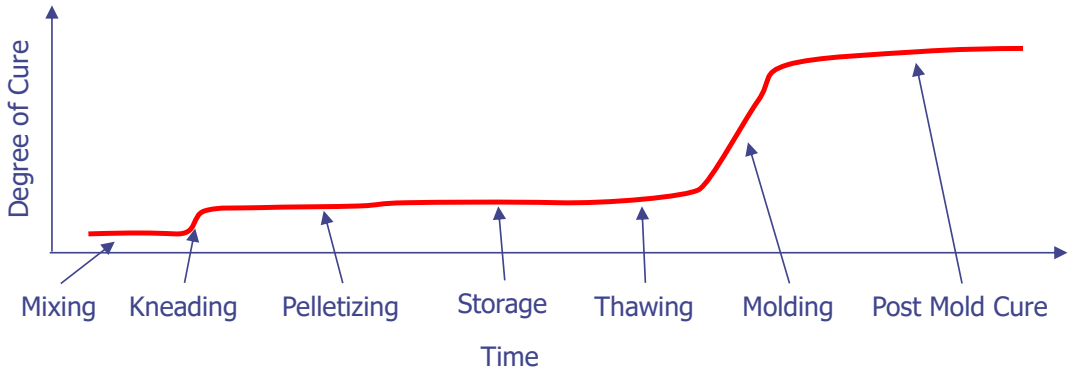


Figure 4- Graph showing the relative degree of curing based on transfer molding process steps.

Warpage can be a problem during both the mold injection and the curing process, so engineers in recent years have invested some time and effort modeling these effects. These simulation images in Figure 5 show examples of both cure-induced warpage, and thermal-induced warpage.

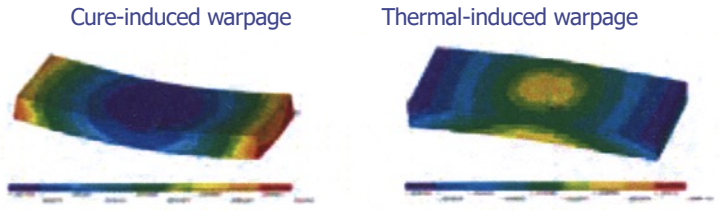


Figure 5- Simulation results showing cure-induced warpage (left) and thermally-induced warpage (right).

In next month's Feature Article, we will continue our discussion of transfer molding by focusing on the mold compound manufacturing process, some issues with mold compound materials, and molding advanced packages.

Technical Tidbit – Warpage Modeling for Substrates

This month's Technical Tidbit covers warpage modeling for substrates. Warpage is a key concern in advanced packages. The differences in Coefficients of Thermal Expansion, the hardness, or Young's Modulus of the materials, and the processing and application conditions can lead to warpage that lowers overall yield and creates reliability issues.

Figure 1 shows an example of measured warpage on a component during the solder reflow process at an assembly-test site. The sample goes from a convex warpage to a concave warpage, and back to convex as the component temperature rises and falls during the solder reflow process, from 25ºC to 260ºC and back. Notice that there is a wide degree of variability measured in the samples, as evidenced by the vertical lines and data points. Traditional modeling has a difficult time handling natural variations, like differences in layer thicknesses, the variability of the weave in an FR-4 substrate, and the impact of die standoffs.

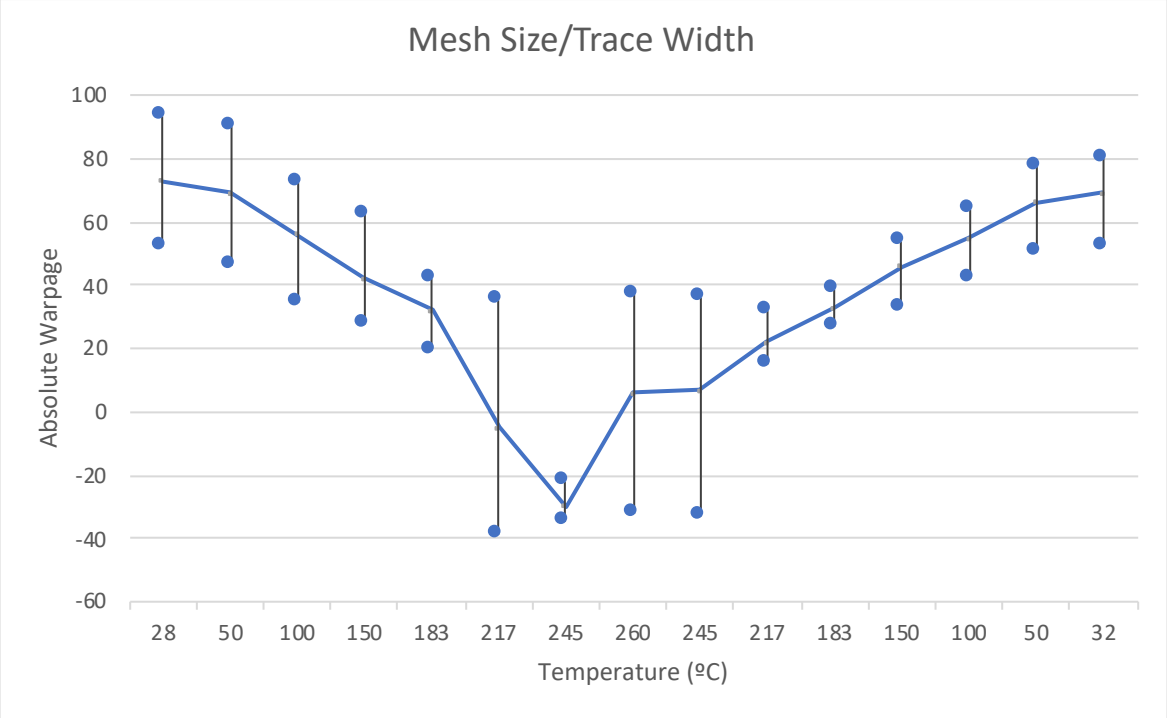
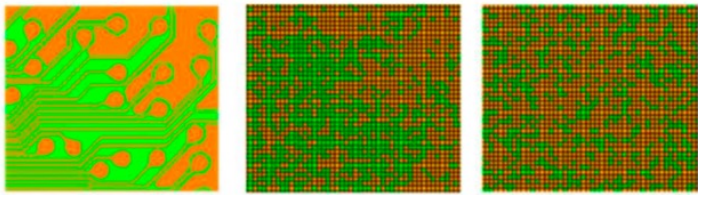


Figure 1- Experimentally measured warpage data on a molded package undergoing the solder reflow process.

One technique for improved modeling of warpage on a finer level is trace layer modeling. In trace layer modeling, one can define a finite element analysis mesh grid, and then identify which blocks in the grid contain predominately copper and which blocks in the grid contain predominately polymers. This is done as zones, and by layers. The number of copper layers and their positioning is often referred to by the term "stack up" in the modeling world, and we will use that term in our article as well. We show an example of this in Figure 2.

Layer-by-layer model capturing layer stack up



Trace mapping
(FEA mesh grid removed)

Zone Cu %

Layer Cu %

Figure 2- Warpage modeling approaches. Layer-by-layer model for substrate core and interconnect stack (top). Copper pattern in-plane models (bottom).

To account for the copper stack-up imbalance and thickness asymmetry, engineers will sometimes perform substrate layer-by-layer modeling with matched layer thickness and metal layer copper area density, like we show in Figure 2 (top). Each metal layer can be simulated with the three-level copper pattern in-plane models as shown in Figure 2 (bottom).

On the left in Figure 2 at the bottom is trace-mapping. In this model, the metal layer is modeled with an extremely fine Finite Element Analysis, or FEA, grid pattern. This grid pattern would have features sizes well below that of the copper trace widths and spacings. Each element in the grid is assigned to a copper or non-metal material based on the local material mapping.

At the center in Figure 2 at the bottom is the Zone Copper % model. In this model, each metal layer is divided into an array of zones. Each element within a zone is assigned either as a copper or non-metal material through a randomization algorithm. Within each zone, the copper area density matches the real design.

At the right in Figure 2 at the bottom is the Layer Copper % model. In this model, the metal layer element material assignment algorithm is the same as that used in the Zone Copper % model. It is equivalent to treating the metal layer as a single zone.

Next, let's discuss which model performs the best at simulating warpage in real applications.

One can then perform finite element analysis using the three different models to determine a normalized warpage.

The graph in Figure 3 shows the warpage dependence on the FEA mesh from this analysis method. The blue data are the results of the trace mapping simulation, the orange data are the results of the Layer Copper % method simulation, and the gray data are the results of the Zone Copper % method. The warpage magnitudes are normalized by that of the best-case Trace-mapping method. The in-plane FEA element mesh size is normalized by the copper trace width.

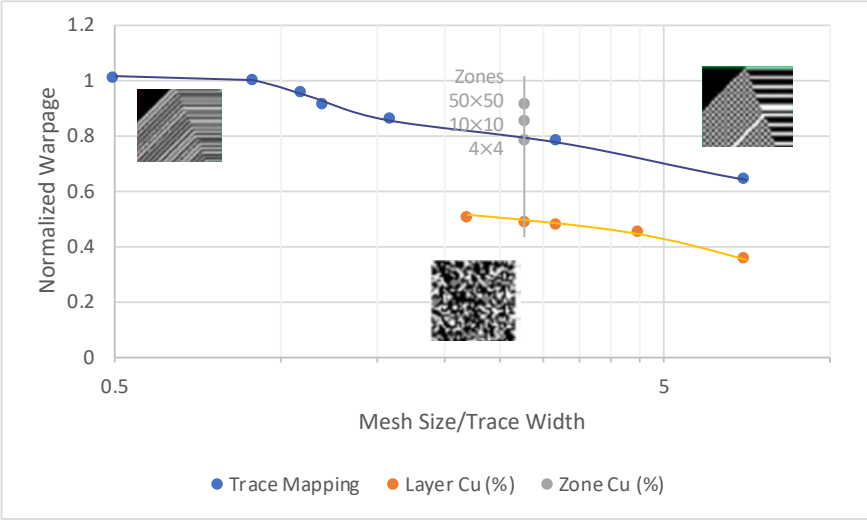


Figure 3- Modeling results for the three warpage models.

Both the Trace-mapping and Layer Copper % methods show high mesh dependency but they saturate asymptotically at different mesh sizes. The warpage by Layer Copper % method converges quickly at moderate mesh sizes. To capture the substrate's true deformation using the Trace-mapping method, the mesh size needs to be refined to be less than the trace width. Coarser meshes than trace width causes the trace aliasing as shown in small inset image on the right in Figure 3.

The Layer Copper % can only capture 50% of the total deformation at the best. However, the Zone Copper % method shows more than 90% of the total deformation with exactly the same level of computation cost as the Layer Copper % method. Moreover, with the moderate array of zones (>20x20) in the layer, the ability to model the deformation by the Zone Copper % method is much better than Layer Copper % method. For this particular package, metal-layer imbalance contributes about 50% of the total deformation. Approximately 40% of the deformation is caused by copper inhomogeneity in the layers. Trace anisotropy only accounts for slightly more than 5% of the total deformation. In this example, the Zone Copper % method shows significant advantages over Layer Copper % method and is sufficient for modeling the substrate warpage, as well as packages using a substrate.

In conclusion, modeling and simulation can provide some insight into the warpage issues associated with complex packaged components. The Zone Copper % method is one technique for modeling warpage that can be done without the expensive computational resources required for a more standard Trace layer modeling approach. Although modeling and simulation can be helpful, there is still significant variability in warpage under real-world processing conditions, due to factors such as layer thicknesses, weave variability, and die standoffs. Clearly, there is room for further improvement in terms of accurately modeling warpage and mechanical stresses, especially in today's complex 3D Heterogenous Integration devices.

Ask The Experts

Q: In Rapid Therma Processing (RTP) are the gases preheated before entering the chamber?

A: Most RTP systems control the gas temperatures through a proper gas inlet design, and showerhead design. The temperature can also be indirectly controlled by rotating the wafer in-situ to minimize gas flow cooling effects, or by reducing the gas flow rate. In general, heating of the gases would be something that process development engineers would characterize during unit process development. Reaction rates of gases, as well as dissociation rates of gases, are generally exponentially dependent upon temperature, so these reactions need to be understood and characterized during process development. Some Computational Fluid Dynamics (CFD) simulation tools can model these types of effects.

Q: How many wafers can you process using Physical Vapor Deposition before needing to replace the target?

A: There are several factors that affect target life. The first is the target material. Different materials erode at different rates during sputtering or evaporation. Harder materials like tungsten or titanium carbide will last longer than softer materials like aluminum or copper. The second is deposition parameters. Higher sputtering power or longer deposition times will consume the target more quickly. The third is film thickness. Thicker films require more material to be deposited, leading to faster target erosion. The fourth is wafer size. The number of wafers that can be processed per target is also related to the size of the wafers being used. Larger wafers will require more material to be deposited, potentially reducing the number of wafers that can be processed before the target needs to be replaced. For example, a large sputtering target could be expected to last for several thousand wafers or more, depending on the factors mentioned above. However, a smaller target or a target being used for a very demanding process (e.g., thick film deposition with high throughput) might last for only a few hundred wafers before it needs to be replaced.

Course Spotlight: FAILURE AND YIELD ANALYSIS

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Failure and Yield Analysis*** is a 4-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants will learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis**. Participants will learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.

2. **The Tools and Techniques**. Participants will learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.

3. **Case Histories**. Participants will identify how to use their knowledge through the case histories. They will learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. This course will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. This course will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. This course will offer a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

DAY 1

1. Introduction

2. Failure Analysis Principles/Procedures
   a. Philosophy of Failure Analysis
   b. Flowcharts

3. Gathering Information

4. Package Level Testing
   a. Optical Microscopy
   b. Acoustic Microscopy
   c. X-Ray Radiography
   d. Hermetic Seal Testing
   e. Residual Gas Analysis

5. Electrical Testing
   a. Basics of Circuit Operation
   b. Curve Tracer/Parameter Analyzer Operation
   c. Quiescent Power Supply Current
   d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
   e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
   f. Automatic Test Equipment
   g. Basics of Digital Circuit Troubleshooting
   h. Basics of Analog Circuit Troubleshooting

DAY 2

6. Decapsulation/Backside Sample Preparation
   a. Mechanical Delidding Techniques
   b. Chemical Delidding Techniques
   c. Backside Sample Preparation Techniques

7. Die Inspection
   a. Optical Microscopy
   b. Scanning Electron Microscopy

8. Photon Emission Microscopy
   a. Mechanisms for Photon Emission
   b. Instrumentation
   c. Frontside
   d. Backside
   e. Interpretation

9. Electron Beam Tools
   a. Voltage Contrast
      i. Passive Voltage Contrast
      ii. Static Voltage Contrast
      iii. Capacitive Coupled Voltage Contrast
      iv. Introduction to Electron Beam Probing
   b. Electron Beam Induced Current
   c. Resistive Contrast Imaging
   d. Charge-Induced Voltage Alteration

COURSE OUTLINE

DAY 3

10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing

11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging

12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing

DAY 4

13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS

14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects

15. Case Histories

Upcoming Courses:

Failure and Yield Analysis - September 29-October 2, 2025 (Mon.-Thurs.) | Phoenix, AZ - $2,195

Silicon Photonics Technology and Applications Webinar - October 22-23, 29-30, 2025 (Wed.-Thurs., Wed-Thurs.) | Online at 8:00 AM-12:00 Noon Pacific Time - $1,295

Wafer Fab Processing - November 3-6, 2025 (Mon.-Thurs.) | Phoenix, AZ - $2,095 until Mon. Oct. 13

Fundamentals of High-Volume Production Test - November 4-5, 2025 (Tues.-Wed.) | Phoenix, AZ - $1,195 until Tues. Oct. 14

Defect-Based Testing - February 19-20, 2026 (Thurs.-Fri.) | Munich, Germany - $1,195 until Thurs. Jan. 29

Wafer Fab Processing - February 23-26, 2026 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Feb. 2

Failure and Yield Analysis - March 2-5, 2026 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Feb. 9

Semiconductor Reliability and Product Qualification - March 9-12, 2026 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Feb. 16

EOS, ESD and How to Differentiate - March 16-17, 2026 (Mon.-Tues.) | Munich, Germany - $1,195 until Mon. Feb. 23

Failure and Yield Analysis - April 13-16, 2026 (Mon.-Thurs.) | San Jose, CA - $2,095 until Mon. Mar. 23

Semiconductor Reliability and Product Qualification - April 20-23, 2026 (Mon.-Thurs.) | San Jose, CA - $2,095 until Mon. Mar. 30

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!